

Compal Confidential

Model Name : VIUS1
File Name : LA-9611P
BOM P/N:

Compal Confidential

M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

www.aitech1.ru
GPU AMD

2012-02-18

REV:0.4

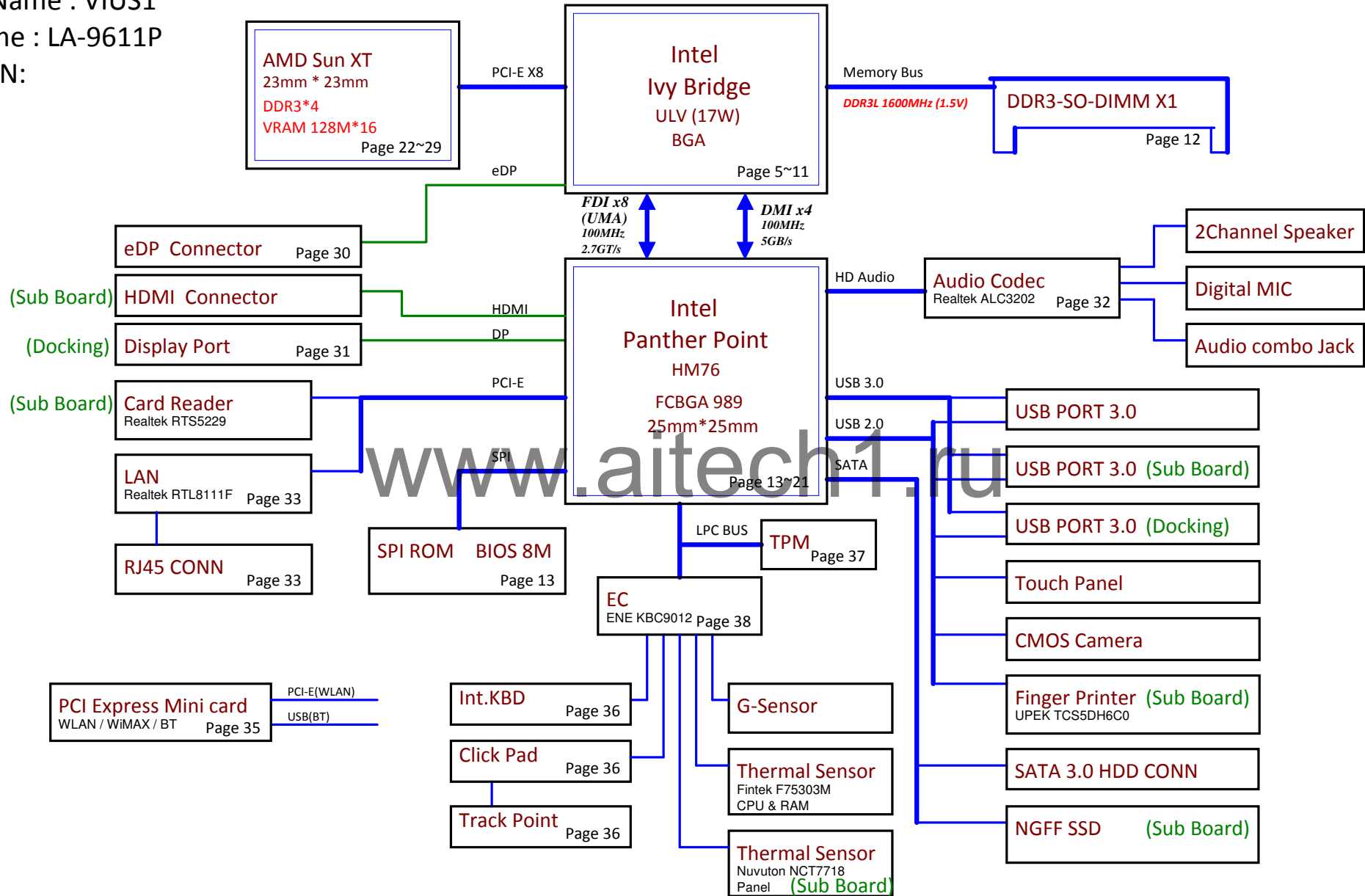
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	Cover Sheet
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Compal Confidential

Model Name : VIUS1

File Name : LA-9611P

BOM P/N:



LA-9611P
DA PCB
DA8000X7000

UCPU1
CPU2@
I5-3337U
SA00006CU20

UCPU1
CPU3@
I3-3227U
SA00006ED20

UCPU1
CPU4@
I5-3437U
SA00006D940

UCPU1
CPU5@
I7-3537U
SA00006D840

UCPU1
CPU6@
Ivy Bridge I7-3537U
SA00006D830

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM (SBA Only)
S0	○	○	○	○	○ M3 Supported
S3	○	○	○	✗	○ M3 Supported
S5 S4/AC	○	○	✗	✗	○ M3 Supported
S5 S4/ Battery only	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist	✗	✗	✗	✗	

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB 3.0 Port (I/O Board)
		1	USB 3.0 Port (MB)
	UHCI1	2	USB 3.0 Port (Docking)
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Touch Panel
		9	(Test point)
	UHCI5	10	Mini Card (WLAN/BT)
		11	FPR
	UHCI6	12	
13			

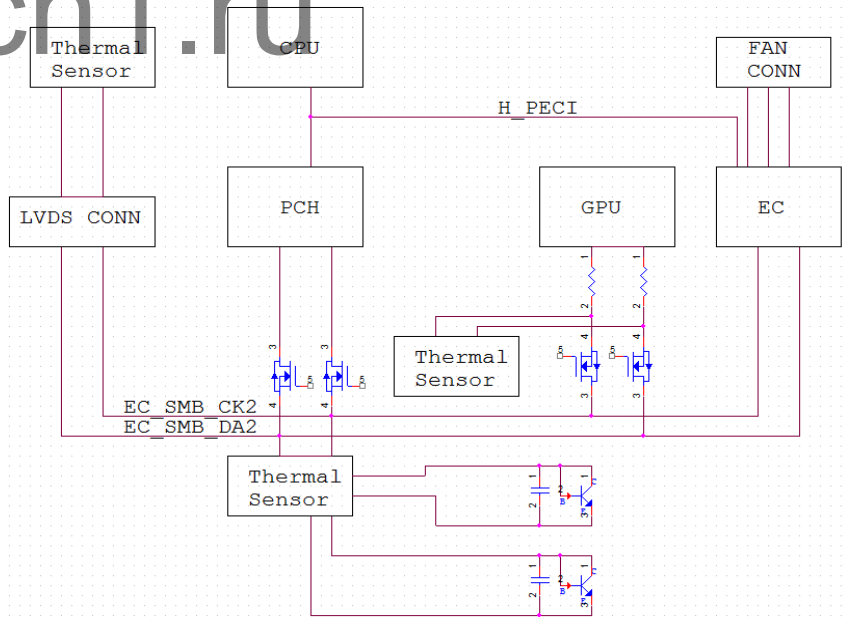
[illegible]

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor Fintek F75303M	1001_101xb

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X



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MB Bottom view



FIDUCIAL_C40M80

FIDUCIAL_C40M80

FIDUCIAL_C40M80

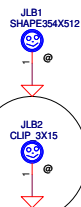
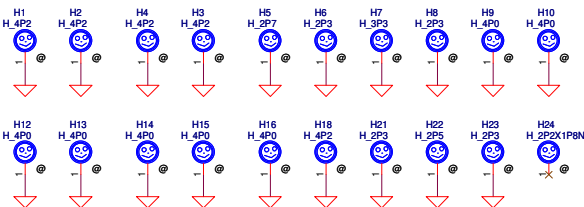
FIDUCIAL_C40M80

PCH

GPU

RAM

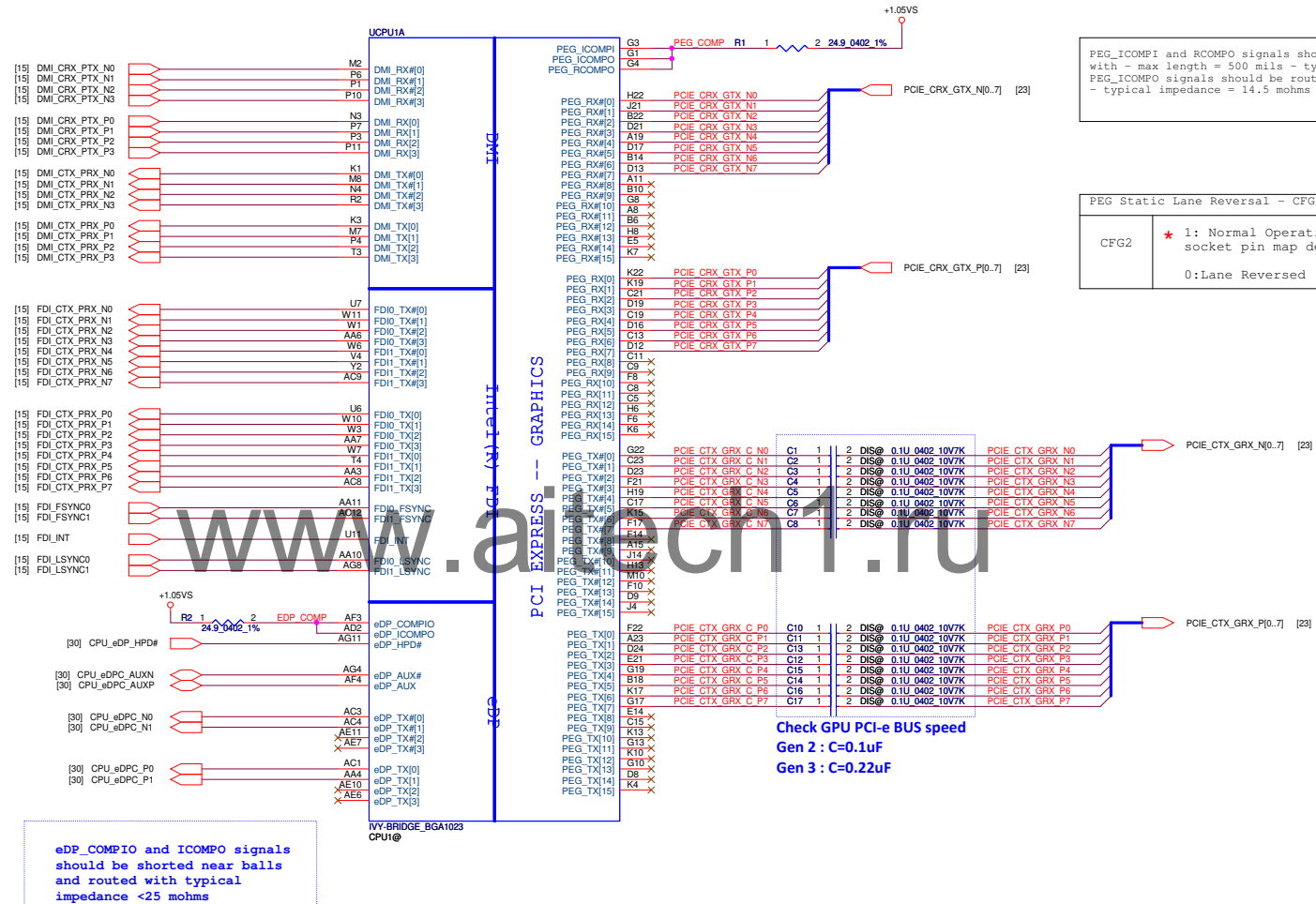
CPU

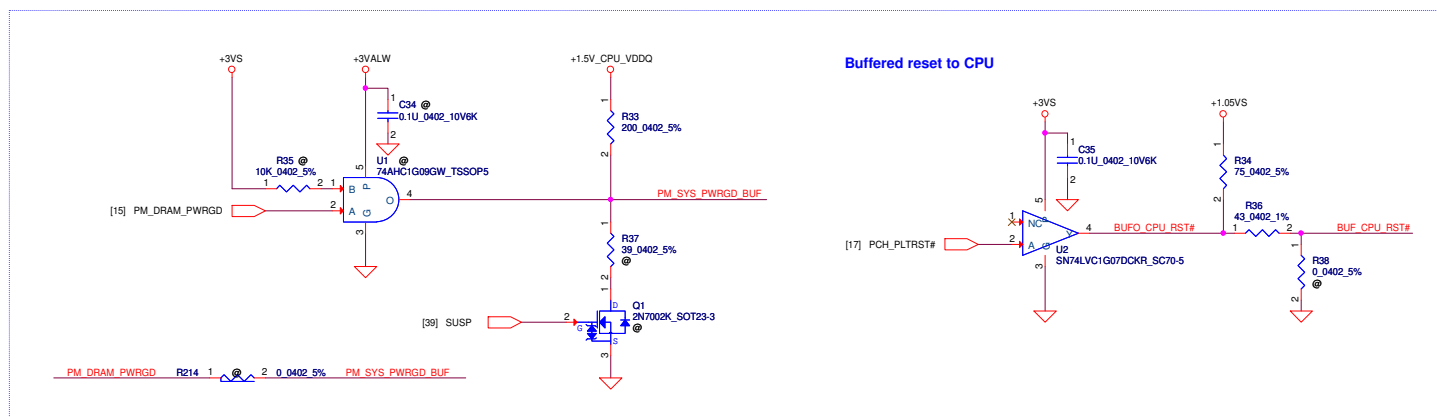
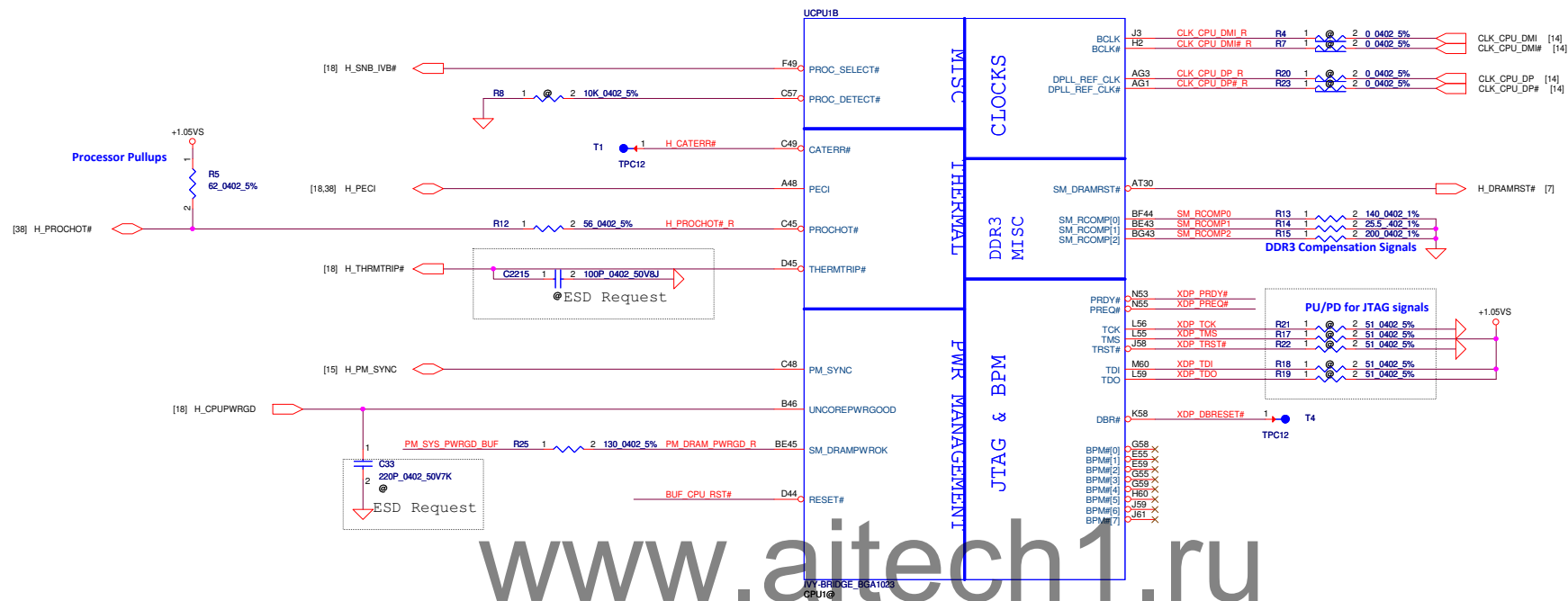


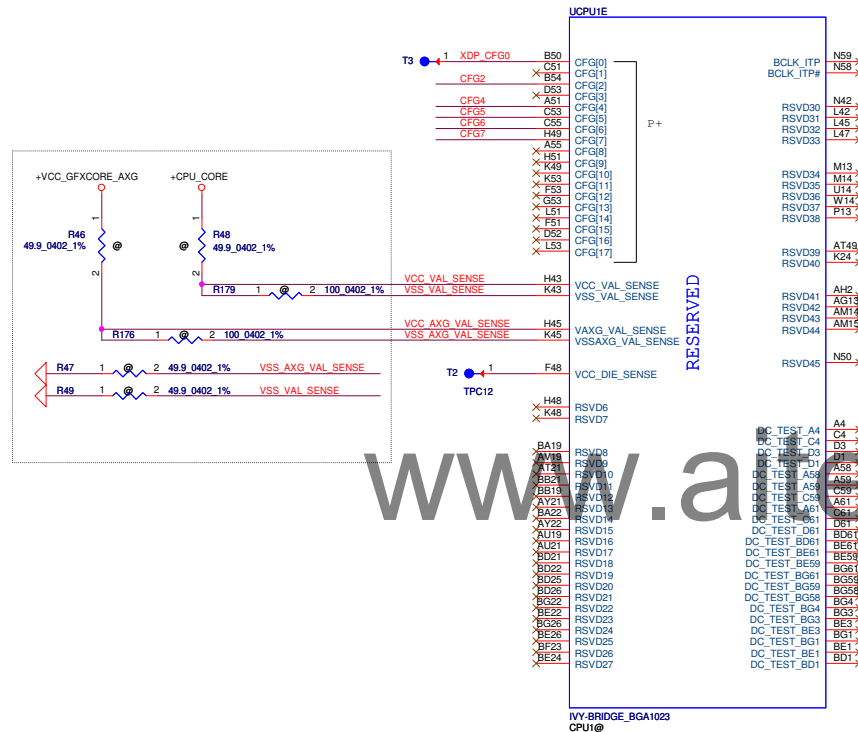
RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
M_PWR_ON
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI



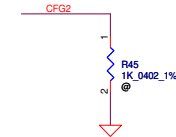
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				LA-9611P	





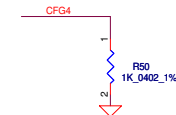


CFG Straps for Processor



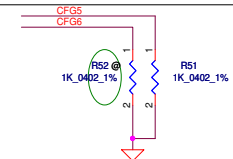
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
------	---



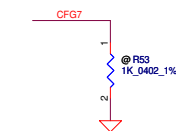
Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
------	---



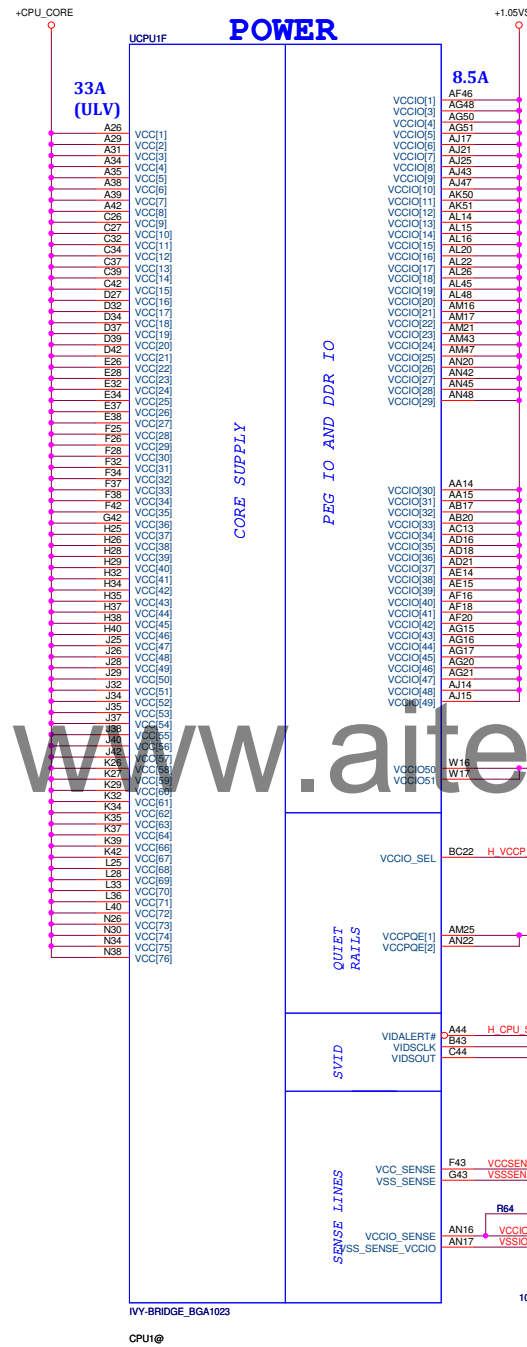
PCIe Port Bifurcation Straps

CFG[6:5]	<p>00 = 1 x8, 2 x4 PCI Express*</p> <p>01 = reserved</p> <p>★ 10 = 2 x8 PCI Express*</p> <p>11 = 1 x16 PCI Express*</p>
----------	---



PEG DEFER TRAINING

CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
------	--



Chief-River platforms
VCCIO_SEL = pulled high

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

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[48] VCC_AXG_SENSE
[48] VSS_AXG_SENSE

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Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

POWER

UCPU1G
(ULV GT2)

AA46 VAXG[1]
AB47 VAXG[2]
AB50 VAXG[3]
AB51 VAXG[4]
AB52 VAXG[5]
AB53 VAXG[6]
AB55 VAXG[7]
AB56 VAXG[8]
AB58 VAXG[9]
AC61 VAXG[10]
AD47 VAXG[11]
AD48 VAXG[12]
AD50 VAXG[13]
AD51 VAXG[14]
AD52 VAXG[15]
AD53 VAXG[16]
AD55 VAXG[17]
AD56 VAXG[18]
AD58 VAXG[19]
AE46 VAXG[20]
AE48 VAXG[21]
AE49 VAXG[22]
P47 VAXG[23]
P48 VAXG[24]
P50 VAXG[25]
P51 VAXG[26]
P52 VAXG[27]
P53 VAXG[28]
P55 VAXG[29]
P56 VAXG[30]
P61 VAXG[31]
T48 VAXG[32]
T58 VAXG[33]
T59 VAXG[34]
T61 VAXG[35]
T62 VAXG[36]
V47 VAXG[37]
V48 VAXG[38]
V49 VAXG[39]
V50 VAXG[40]
V51 VAXG[41]
V52 VAXG[42]
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W53 VAXG[50]
W55 VAXG[51]
W56 VAXG[52]
W61 VAXG[53]
Y48 VAXG[54]
Y61 VAXG[55]
Y61 VAXG[56]

DDR3 - 1.5V RAILS

QUIET RAILS

SA RAIL

VCCSA VID Lines

IVY-BRIDGE_BGA1023

CPU1@

VREF

SA_DIMM_VREFDQ

SB_DIMM_VREFDQ

SM_VREF

AY43 -V SM_VREF_CNT

BE7 -V DDR_REFA_R

BG7 -V DDR_REFB_R

VDDQ[1]

VDDQ[2]

VDDQ[3]

VDDQ[4]

VDDQ[5]

VDDQ[6]

VDDQ[7]

VDDQ[8]

VDDQ[9]

VDDQ[10]

VDDQ[11]

VDDQ[12]

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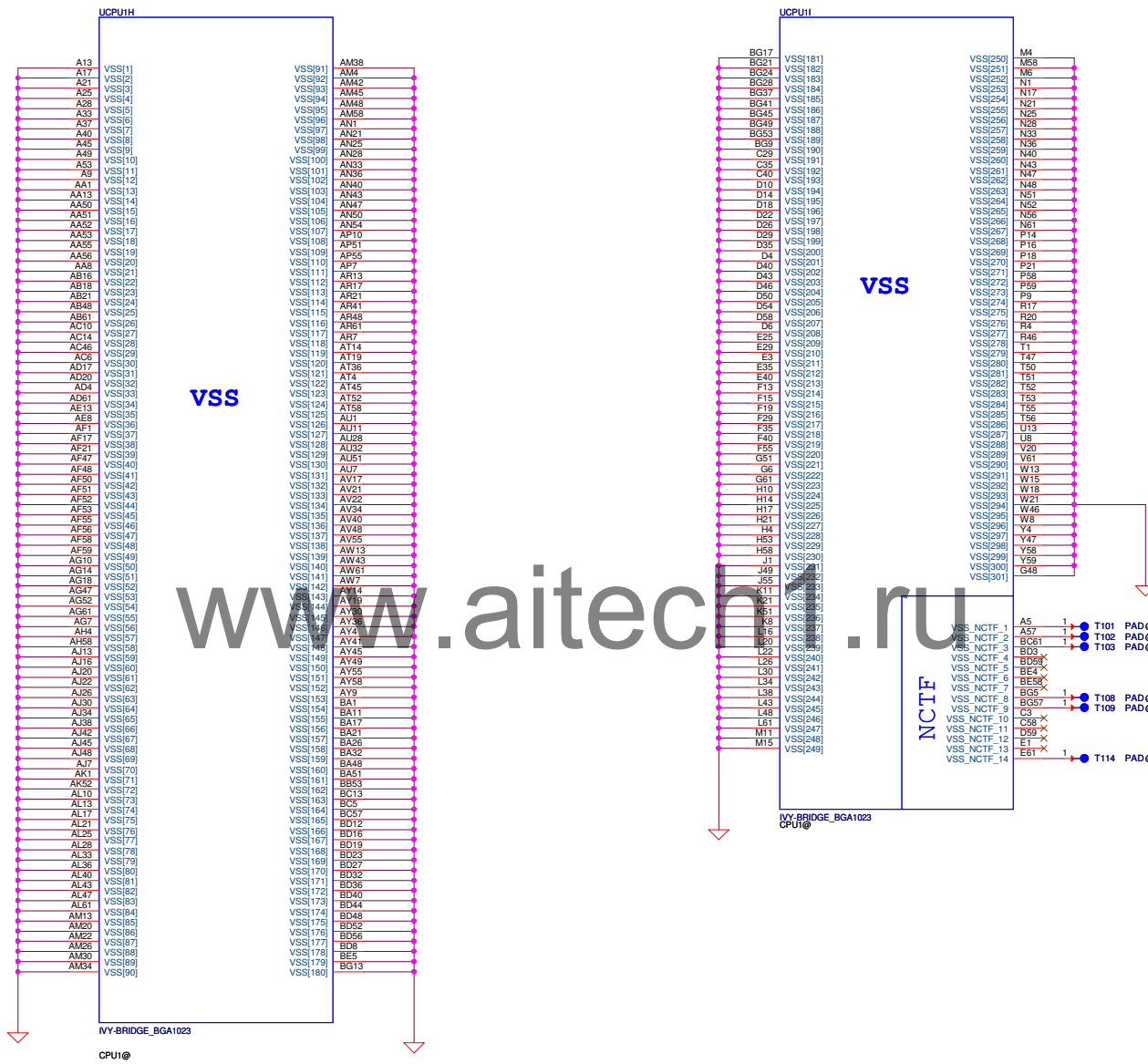
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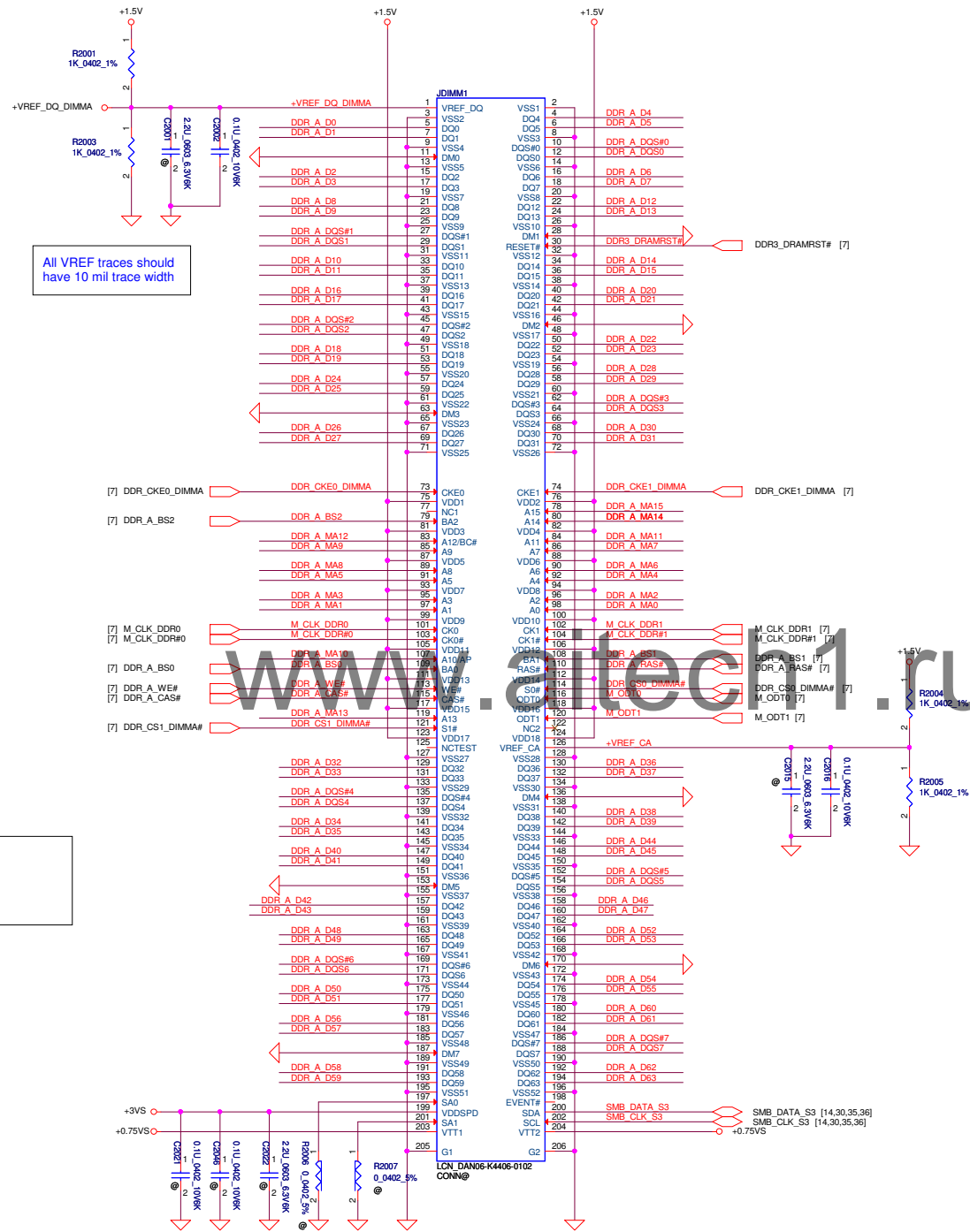
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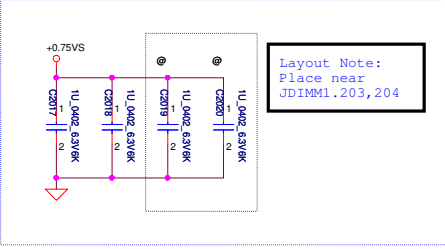
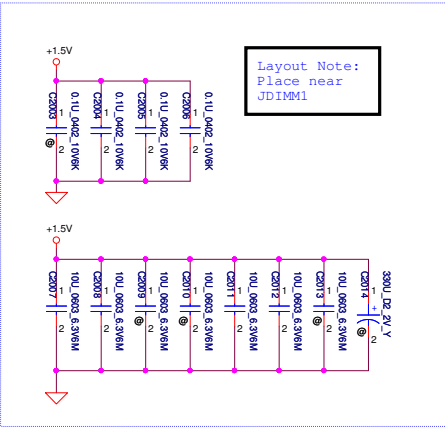
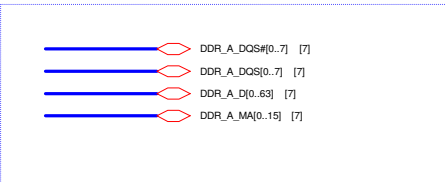




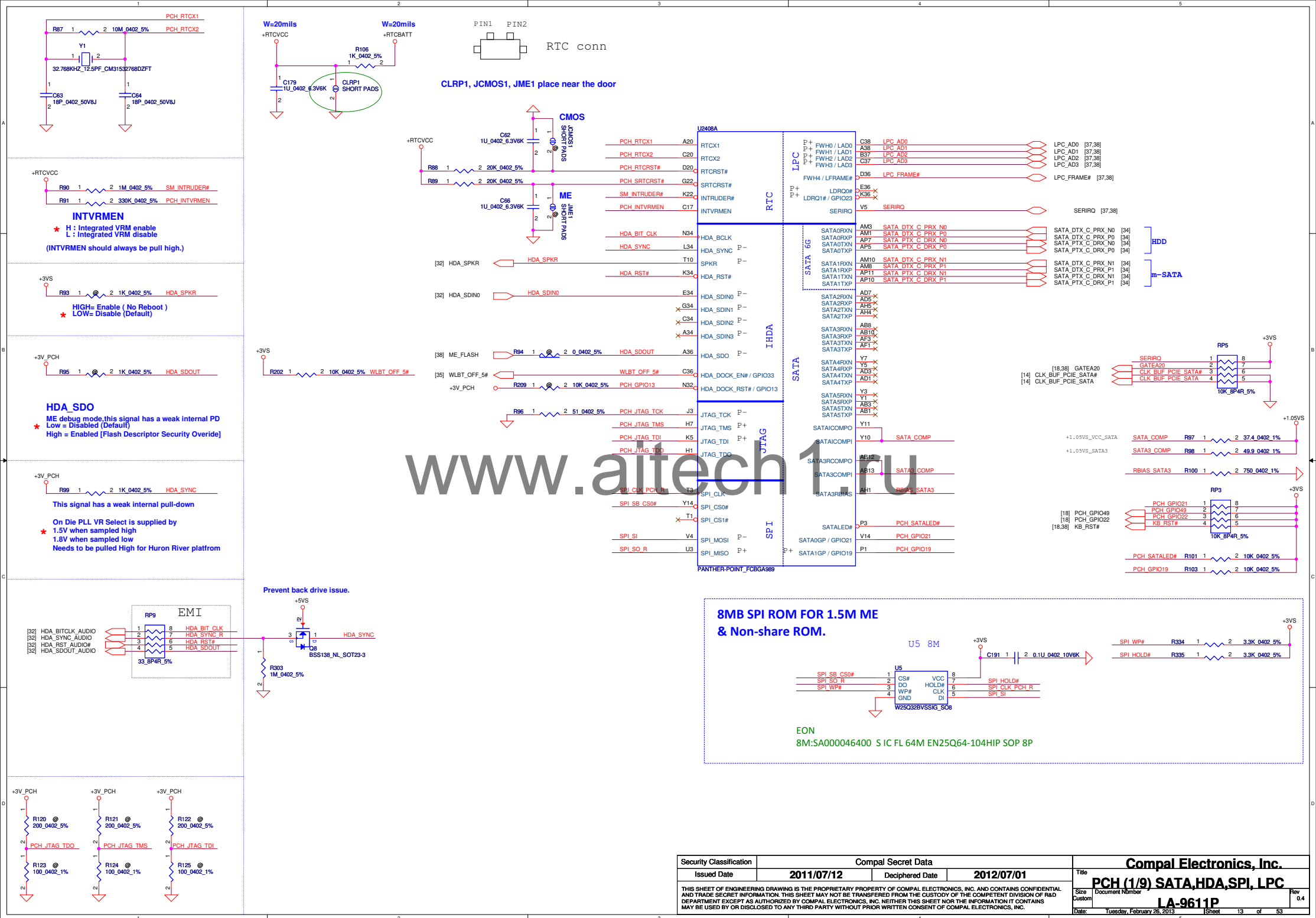
All VREF traces should have 10 mil trace width

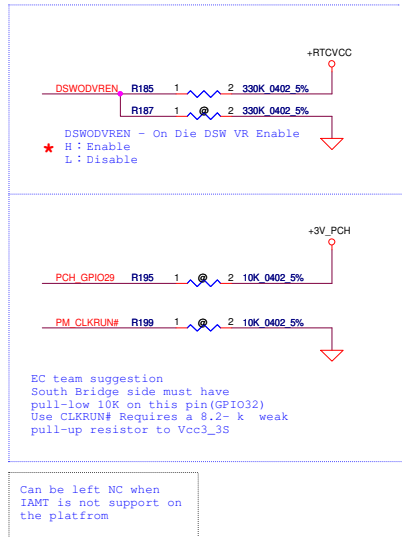
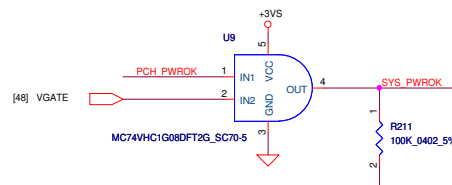
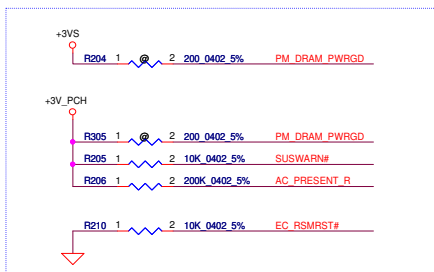
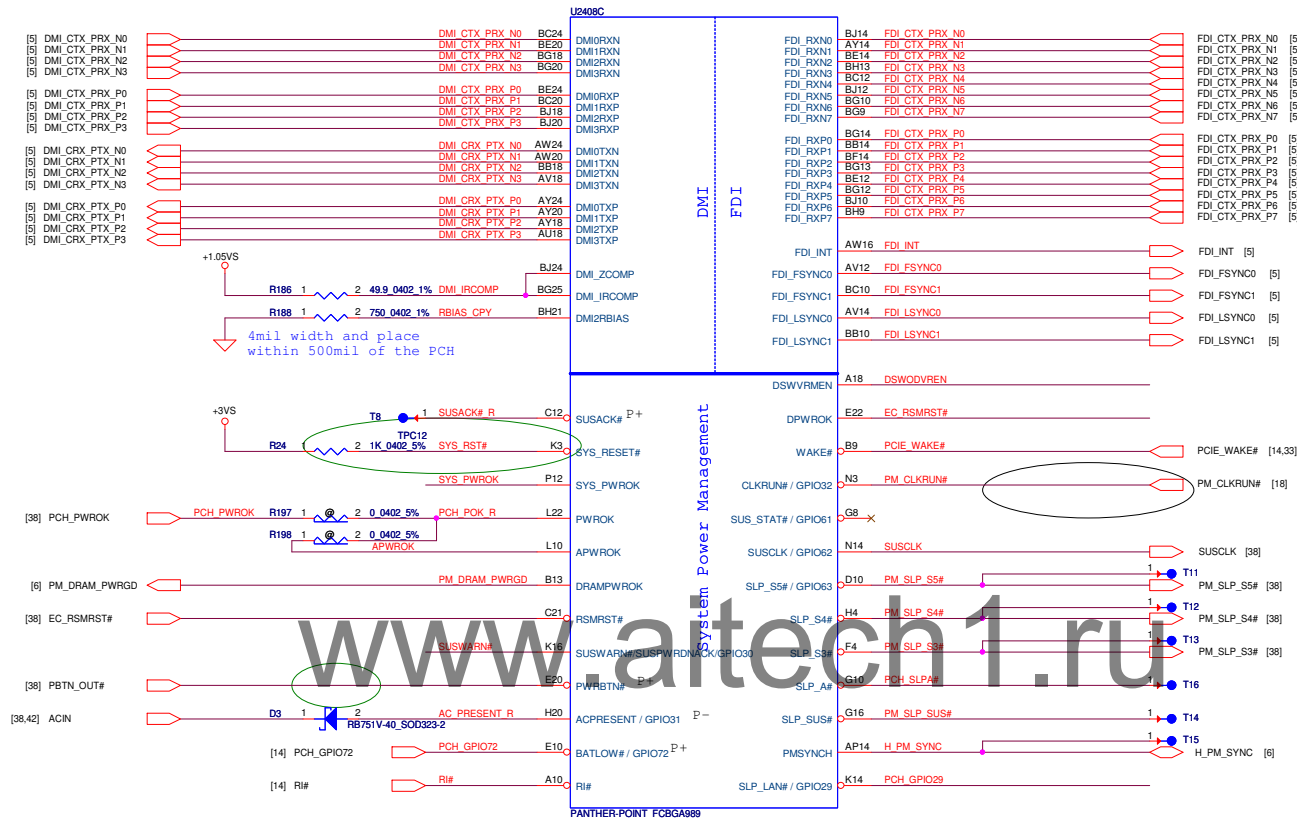
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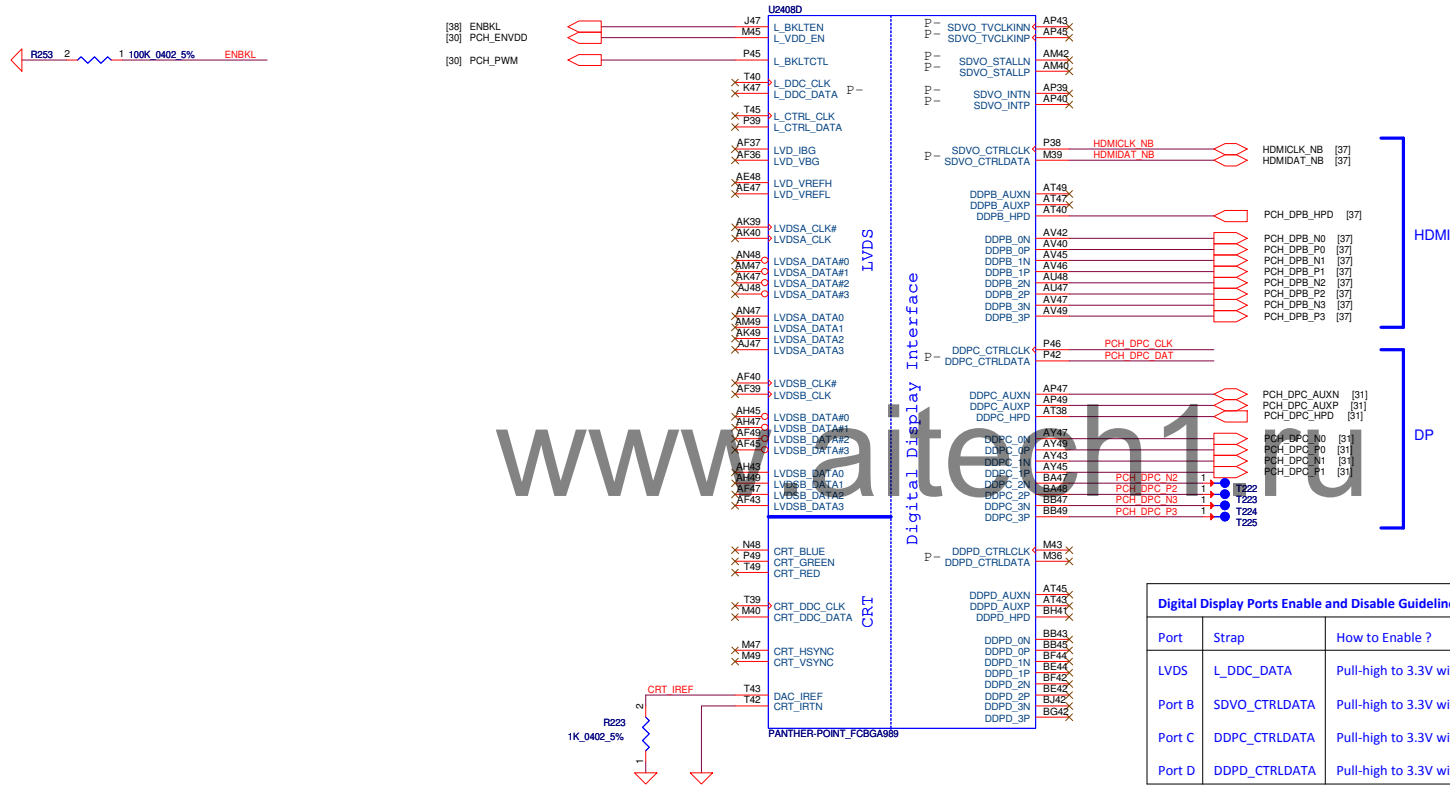


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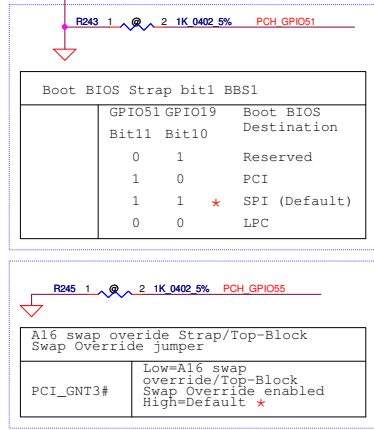




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Digital Display Ports Enable and Disable Guidelines			
Port	Strap	How to Enable ?	How to Disable ?
LVDS	L_DDC_DATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port B	SDVO_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port C	DDPC_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port D	DDPD_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect



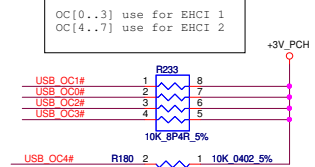
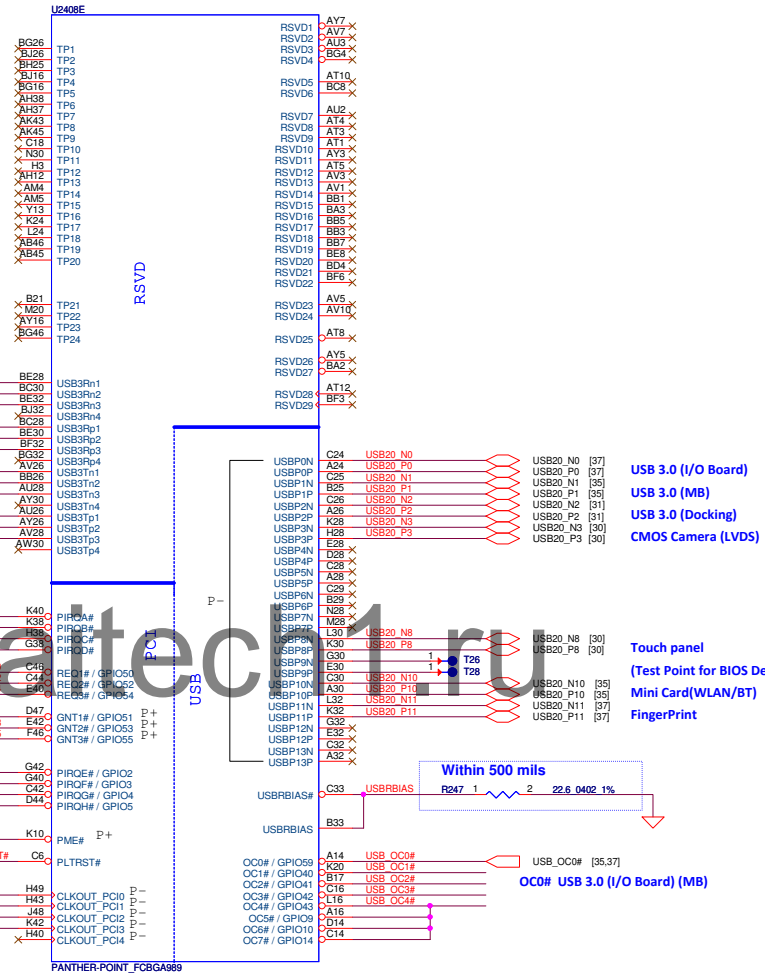
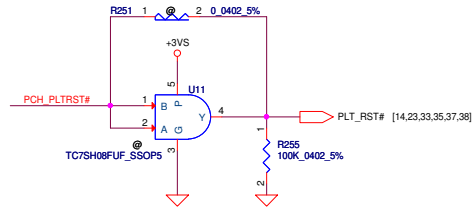
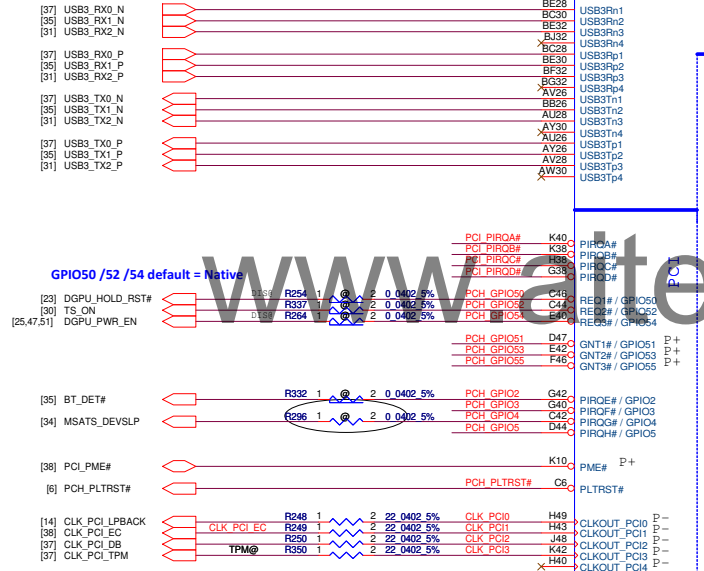
GPIO0#, GPIO1#/GPIO51, GPIO2#/GPIO53, GPIO3#/GPIO55
PCI Grants: The PCH supports up to 4 masters on the PCI bus.

GPIO[3:1]# pins can instead be used as GPIO.

Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.

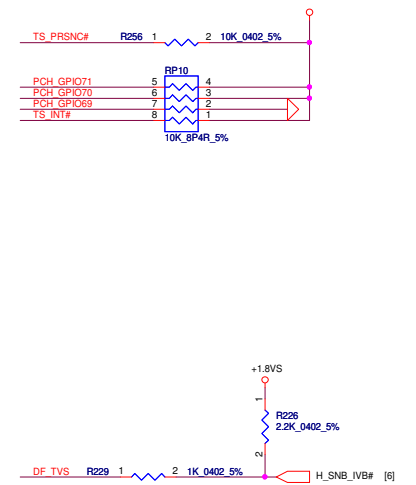
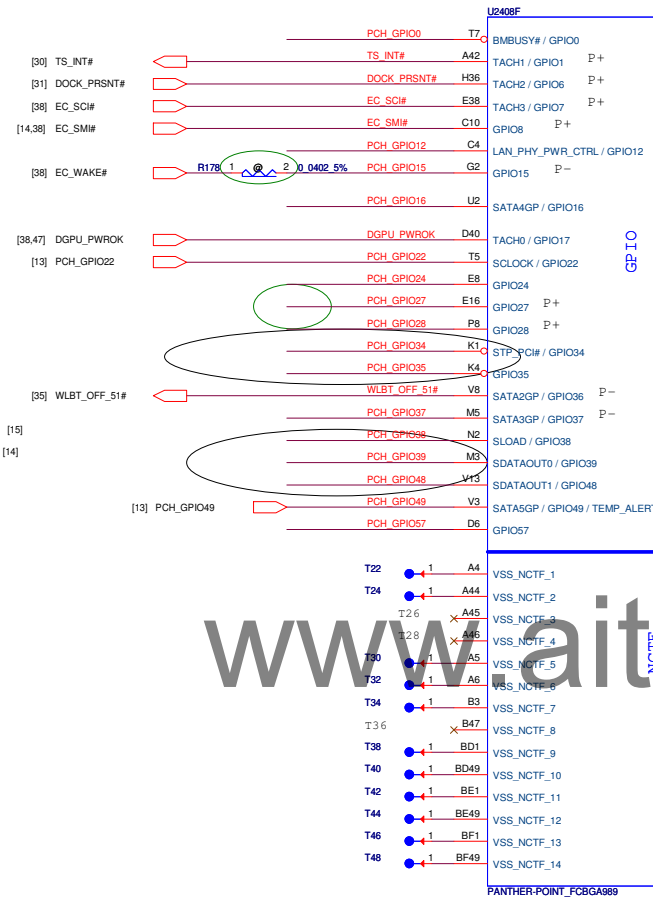
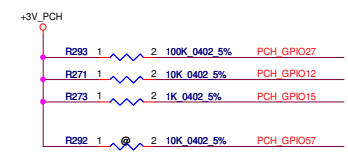
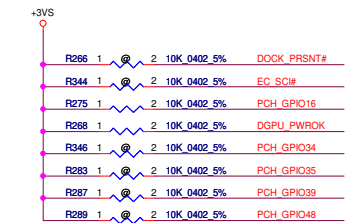
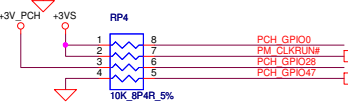
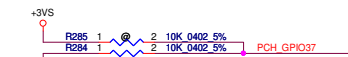
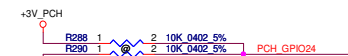
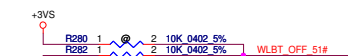
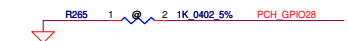
NOTES:

- GPIO[3:1]#/GPIO[55,53,51] are sampled as a functional strap. See Section 2.27 for details.



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

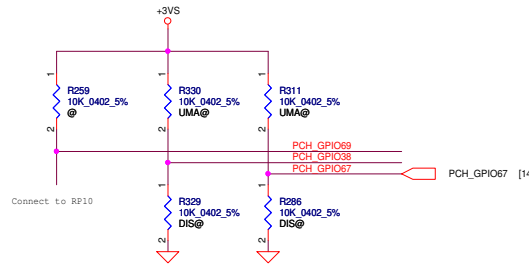
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



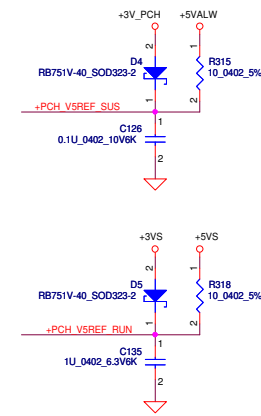
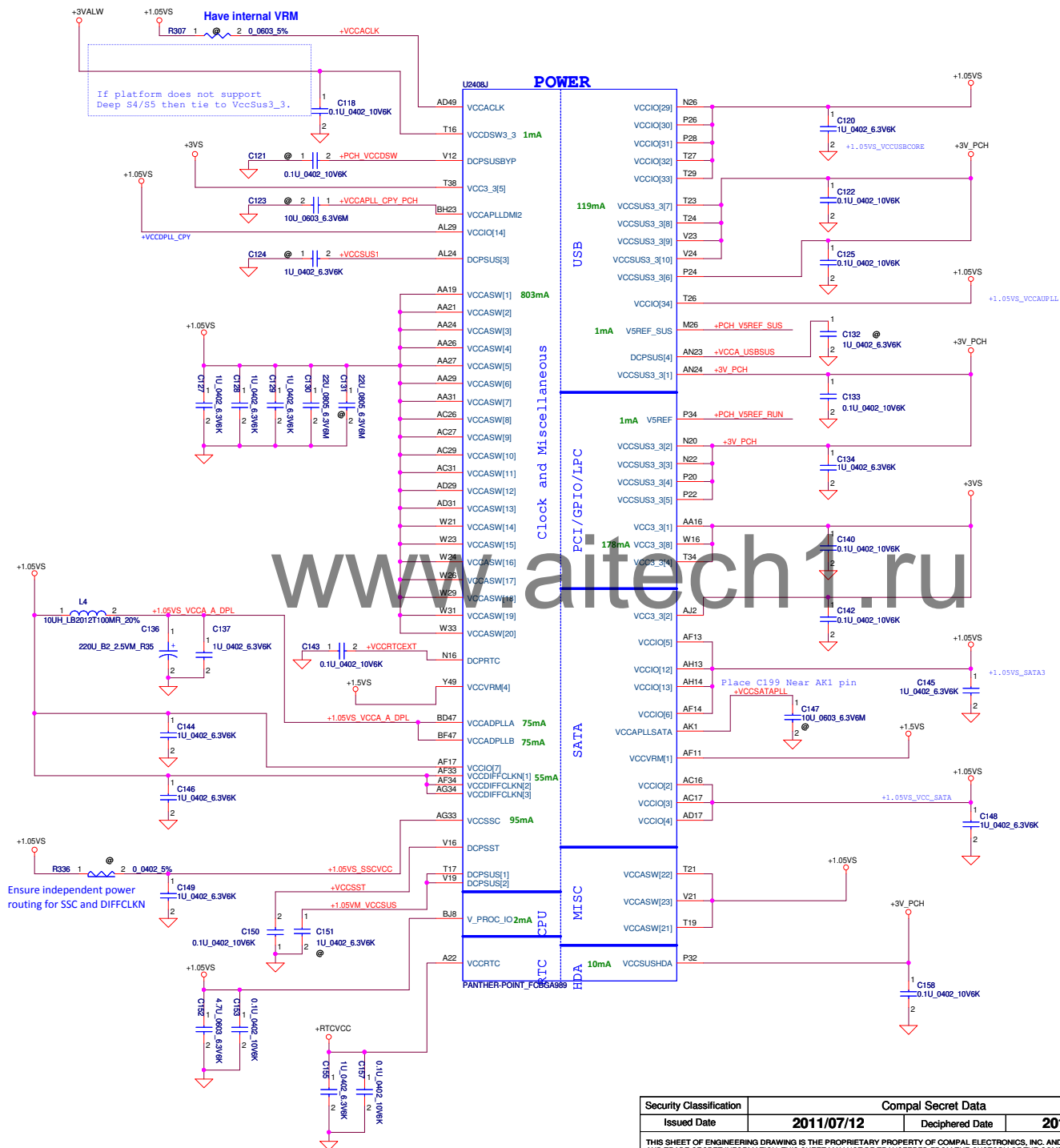
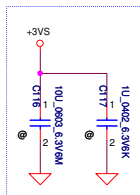
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA




```
VCC3_3 = 266mA detal waiting for newest spe
VCCDMI = 42mA detal waiting for newest spec
```



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						Size	Document Number	Rev
						Custom	LA-9611P	0.4
						Date:	Tuesday, February 26, 2013	Sheet

U2408H		
H5	VSS[0]	AK38
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	VSS[81]
AA3	VSS[3]	VSS[82]
AA33	VSS[4]	VSS[83]
AA34	VSS[5]	VSS[84]
AB11	VSS[6]	VSS[85]
AB14	VSS[7]	VSS[86]
AB39	VSS[8]	VSS[87]
AB4	VSS[9]	VSS[88]
AB43	VSS[10]	VSS[89]
AB5	VSS[11]	VSS[90]
AB7	VSS[12]	VSS[91]
AC2	VSS[13]	VSS[92]
AC19	VSS[14]	VSS[93]
AC21	VSS[15]	VSS[94]
AC24	VSS[16]	VSS[95]
AC33	VSS[17]	VSS[96]
AC34	VSS[18]	VSS[97]
AC48	VSS[19]	VSS[98]
AD10	VSS[20]	VSS[99]
AD11	VSS[21]	VSS[100]
AD12	VSS[22]	VSS[101]
AD13	VSS[23]	VSS[102]
AD19	VSS[24]	VSS[103]
AD24	VSS[25]	VSS[104]
AD26	VSS[26]	VSS[105]
AD27	VSS[27]	VSS[106]
AD33	VSS[28]	VSS[107]
AD34	VSS[29]	VSS[108]
AD36	VSS[30]	VSS[109]
AD37	VSS[31]	VSS[110]
AD38	VSS[32]	VSS[111]
AD39	VSS[33]	VSS[112]
AD4	VSS[34]	VSS[113]
AD40	VSS[35]	VSS[114]
AD42	VSS[36]	VSS[115]
AD43	VSS[37]	VSS[116]
AD45	VSS[38]	VSS[117]
AD46	VSS[39]	VSS[118]
AD8	VSS[40]	VSS[119]
AE2	VSS[41]	VSS[120]
AE3	VSS[42]	VSS[121]
AF10	VSS[43]	VSS[122]
AF12	VSS[44]	VSS[123]
AD14	VSS[45]	VSS[124]
AD16	VSS[46]	VSS[125]
AF16	VSS[47]	VSS[126]
AF19	VSS[48]	VSS[127]
AF24	VSS[49]	VSS[128]
AF26	VSS[50]	VSS[129]
AF27	VSS[51]	VSS[130]
AF29	VSS[52]	VSS[131]
AF31	VSS[53]	VSS[132]
AF38	VSS[54]	VSS[133]
AF4	VSS[55]	VSS[134]
AF42	VSS[56]	VSS[135]
AF46	VSS[57]	VSS[136]
AF5	VSS[58]	VSS[137]
AF7	VSS[59]	VSS[138]
AF8	VSS[60]	VSS[139]
AG19	VSS[61]	VSS[140]
AG2	VSS[62]	VSS[141]
AG31	VSS[63]	VSS[142]
AG48	VSS[64]	VSS[143]
AH11	VSS[65]	VSS[144]
AH3	VSS[66]	VSS[145]
AH36	VSS[67]	VSS[146]
AH39	VSS[68]	VSS[147]
AH40	VSS[69]	VSS[148]
AH42	VSS[70]	VSS[149]
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
AJ19	VSS[73]	VSS[152]
AJ21	VSS[74]	VSS[153]
AJ24	VSS[75]	VSS[154]
AJ33	VSS[76]	VSS[155]
AJ34	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]

PANTHER-POINT_FCBGA989

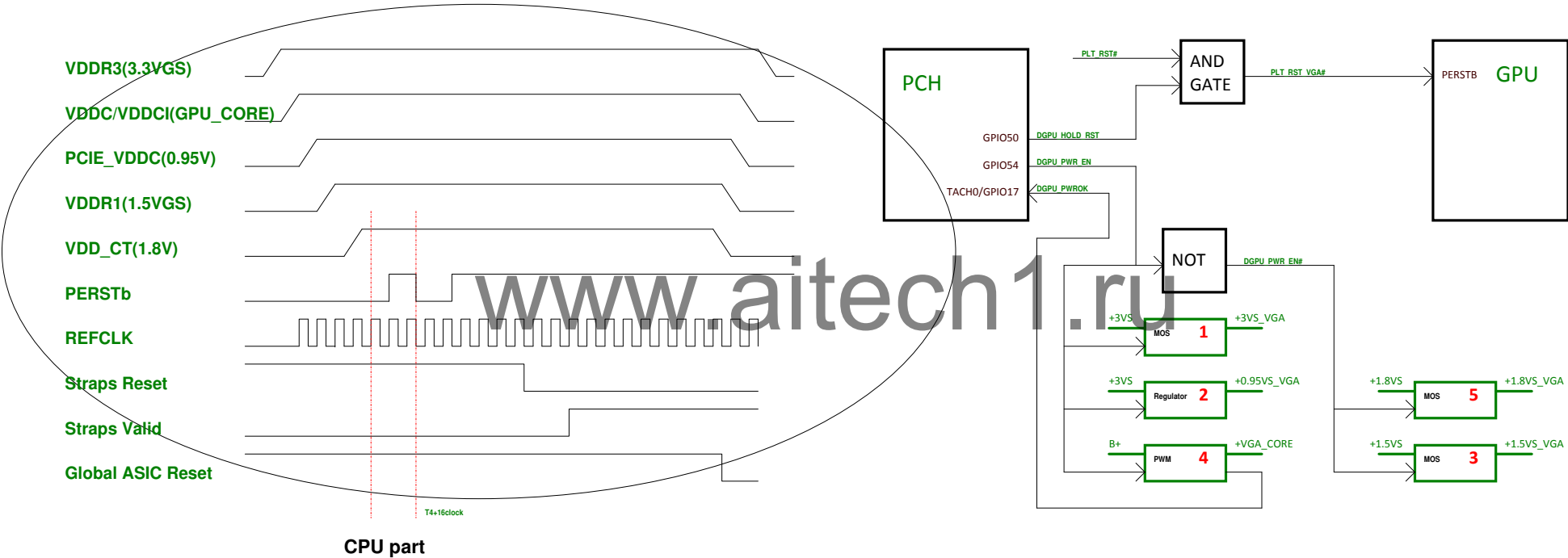
U2408		
AY4	VSS[159]	H46
AY42	VSS[160]	VSS[259]
AY46	VSS[161]	VSS[260]
AY8	VSS[162]	VSS[261]
B11	VSS[163]	VSS[262]
B15	VSS[164]	VSS[263]
B19	VSS[165]	VSS[264]
B23	VSS[166]	VSS[265]
B27	VSS[167]	VSS[266]
B31	VSS[168]	VSS[267]
B35	VSS[169]	VSS[268]
B39	VSS[170]	VSS[269]
B7	VSS[171]	VSS[270]
F45	VSS[172]	VSS[271]
BB12	VSS[173]	VSS[272]
BB16	VSS[174]	VSS[273]
BB20	VSS[175]	VSS[274]
BB22	VSS[176]	VSS[275]
BB24	VSS[177]	VSS[276]
BB28	VSS[178]	VSS[277]
BB30	VSS[179]	VSS[278]
BB38	VSS[180]	VSS[279]
BB4	VSS[181]	VSS[280]
BB46	VSS[182]	VSS[281]
BC14	VSS[183]	VSS[282]
BC16	VSS[184]	VSS[283]
BC2	VSS[185]	VSS[284]
BC22	VSS[186]	VSS[285]
BC26	VSS[187]	VSS[286]
BC32	VSS[188]	VSS[287]
BC34	VSS[189]	VSS[288]
BC36	VSS[190]	VSS[289]
BC40	VSS[191]	VSS[290]
BC42	VSS[192]	VSS[291]
BC48	VSS[193]	VSS[292]
BD42	VSS[194]	VSS[293]
BD5	VSS[195]	VSS[294]
BE22	VSS[196]	VSS[295]
BE26	VSS[197]	VSS[296]
BE40	VSS[198]	VSS[297]
BF10	VSS[199]	VSS[298]
BF12	VSS[200]	VSS[299]
BF16	VSS[201]	VSS[300]
BF20	VSS[202]	VSS[301]
BF22	VSS[203]	VSS[302]
BF24	VSS[204]	VSS[303]
BF26	VSS[205]	VSS[304]
BF28	VSS[206]	VSS[305]
BF30	VSS[207]	VSS[306]
BF38	VSS[208]	VSS[307]
BF40	VSS[209]	VSS[308]
BF8	VSS[210]	VSS[309]
BG17	VSS[211]	VSS[310]
BG21	VSS[212]	VSS[311]
BG35	VSS[213]	VSS[312]
BG44	VSS[214]	VSS[313]
BG8	VSS[215]	VSS[314]
BH11	VSS[216]	VSS[315]
BH15	VSS[217]	VSS[316]
BH17	VSS[218]	VSS[317]
BH19	VSS[219]	VSS[318]
H10	VSS[220]	VSS[319]
BH27	VSS[221]	VSS[320]
BH31	VSS[222]	VSS[321]
BH33	VSS[223]	VSS[322]
BH35	VSS[224]	VSS[323]
BH39	VSS[225]	VSS[324]
BH43	VSS[226]	VSS[325]
BH7	VSS[227]	VSS[326]
B3	VSS[228]	VSS[327]
D12	VSS[229]	VSS[328]
D16	VSS[230]	VSS[329]
D18	VSS[231]	VSS[330]
D22	VSS[232]	VSS[331]
D24	VSS[233]	VSS[332]
D26	VSS[234]	VSS[333]
D30	VSS[235]	VSS[334]
D32	VSS[236]	VSS[335]
D34	VSS[237]	VSS[336]
D38	VSS[238]	VSS[337]
D42	VSS[239]	VSS[338]
D6	VSS[240]	VSS[339]
E18	VSS[241]	VSS[340]
E26	VSS[242]	VSS[341]
G18	VSS[243]	VSS[342]
G20	VSS[244]	VSS[343]
G26	VSS[245]	VSS[344]
G36	VSS[246]	VSS[345]
G48	VSS[247]	VSS[346]
H12	VSS[248]	VSS[347]
H16	VSS[249]	VSS[348]
H22	VSS[250]	VSS[349]
H24	VSS[251]	VSS[350]
H26	VSS[252]	VSS[351]
H30	VSS[253]	VSS[352]
H32	VSS[254]	VSS[353]
H34	VSS[255]	VSS[354]
F3	VSS[256]	VSS[355]

PANTHER-POINT_FCBGA989

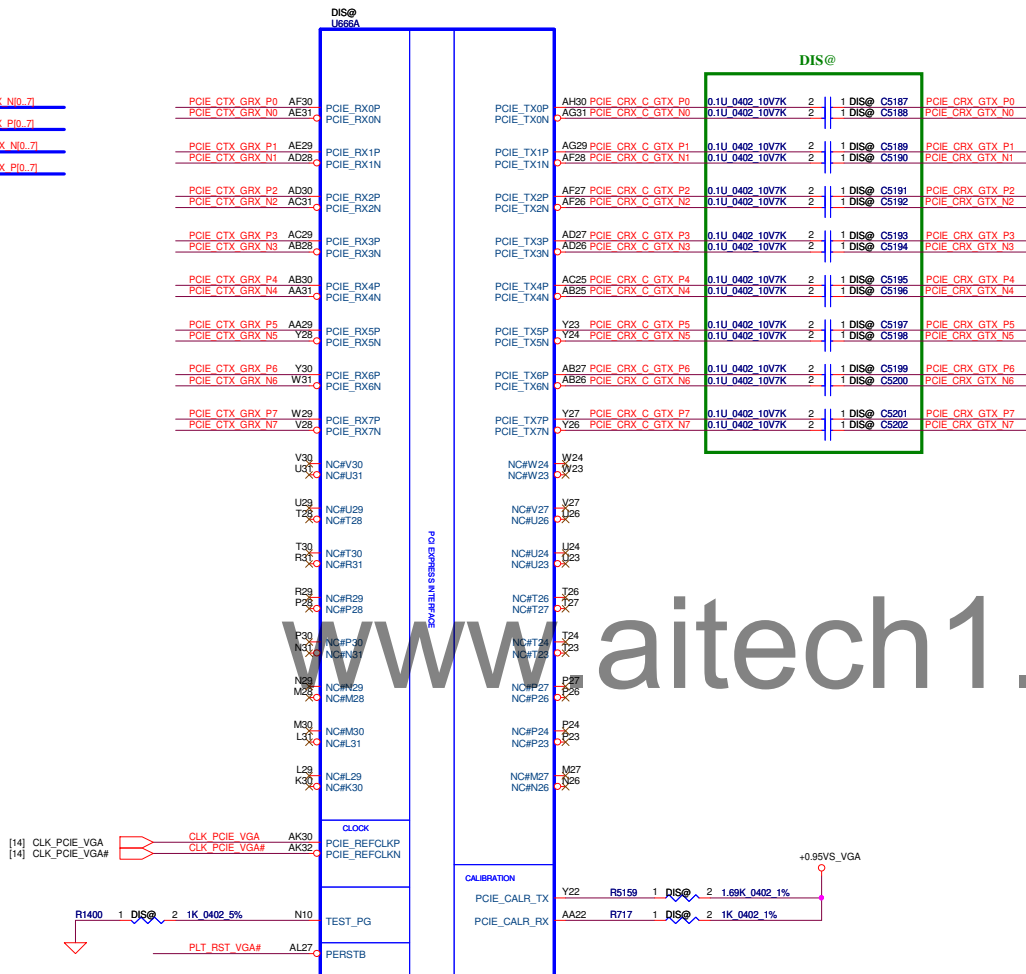
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Size		Document Number		LA-9611P	
Date		Tuesday, February 26, 2013		Rev 0.4	
Sheet		21		of 53	

Power-Up/Down Sequence

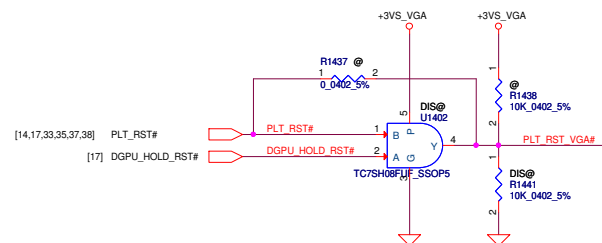
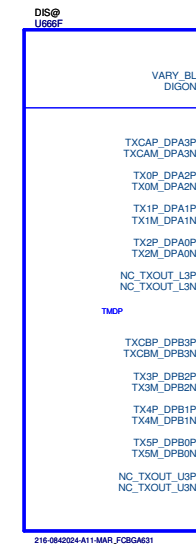
- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- 2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- 3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- 4. For power down, reversing the ramp-up sequence is recommended.



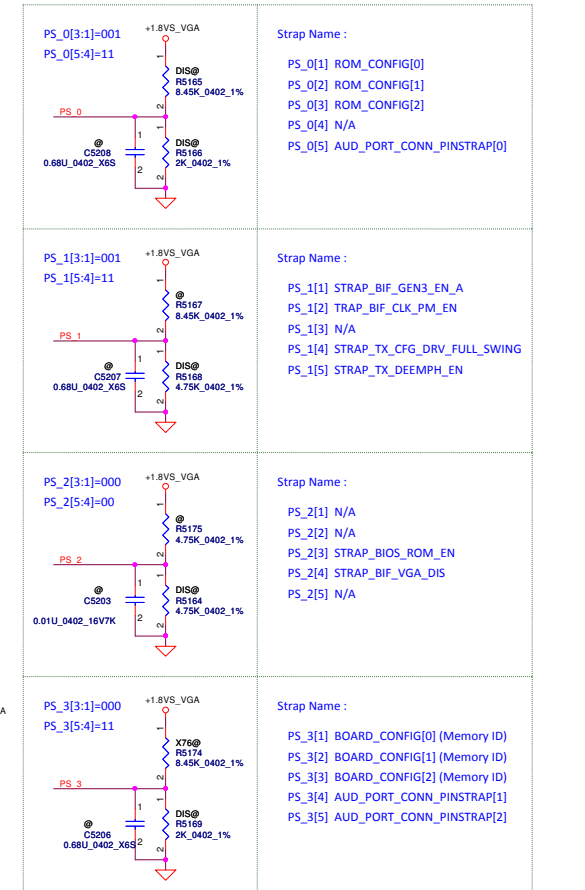
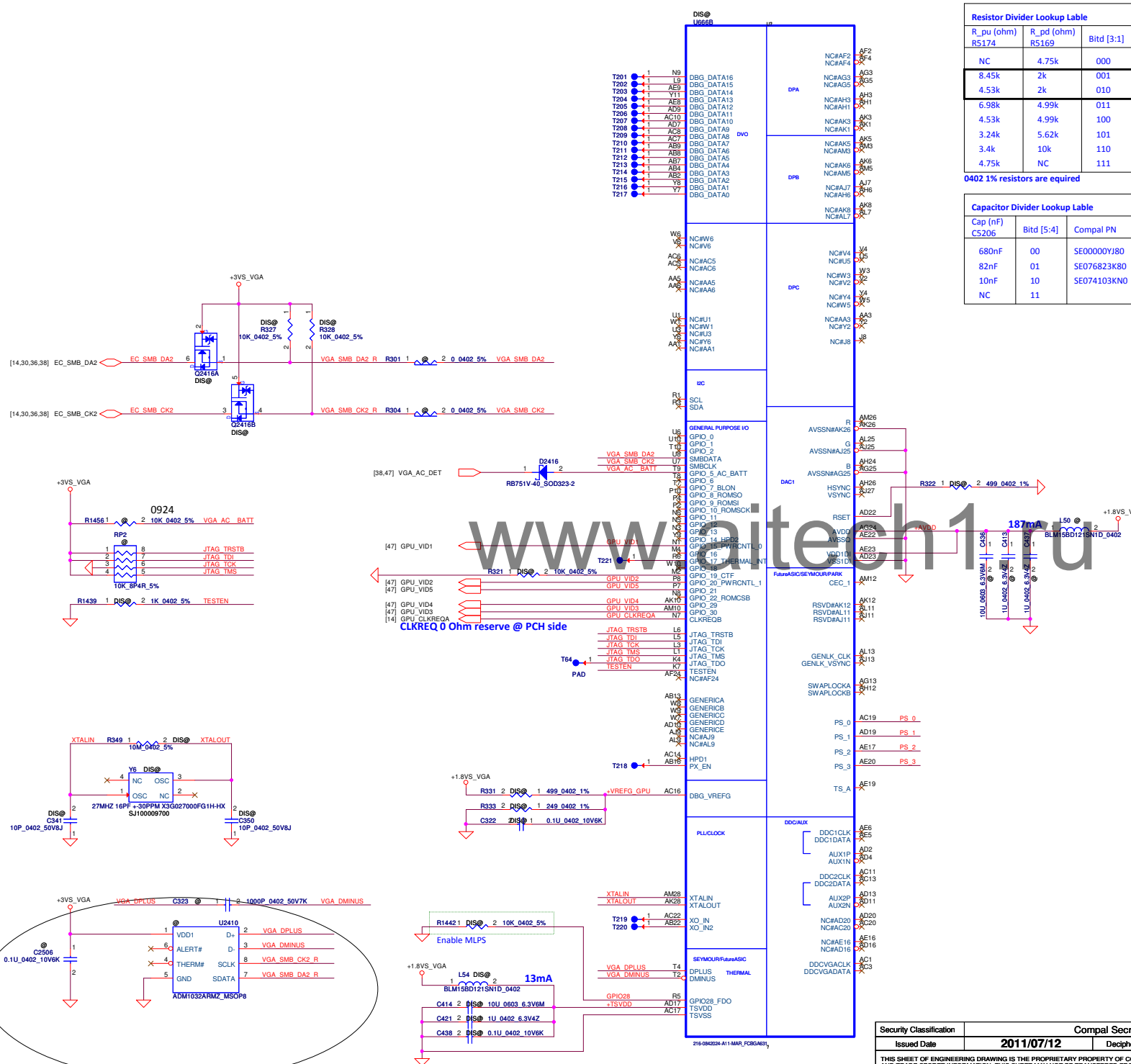
- [5] PCIE_CTX_GRX_N0..7] PCIE_CTX_GRX_N0..7]
- [5] PCIE_CTX_GRX_P0..7] PCIE_CTX_GRX_P0..7]
- [5] PCIE_CRX_GTX_N0..7] PCIE_CRX_GTX_N0..7]
- [5] PCIE_CRX_GTX_P0..7] PCIE_CRX_GTX_P0..7]



No Use GPU Display Port output

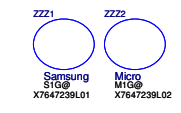


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				Date	Rev
				Tuesday, February 26, 2013	04
				Sheet	23 of 53

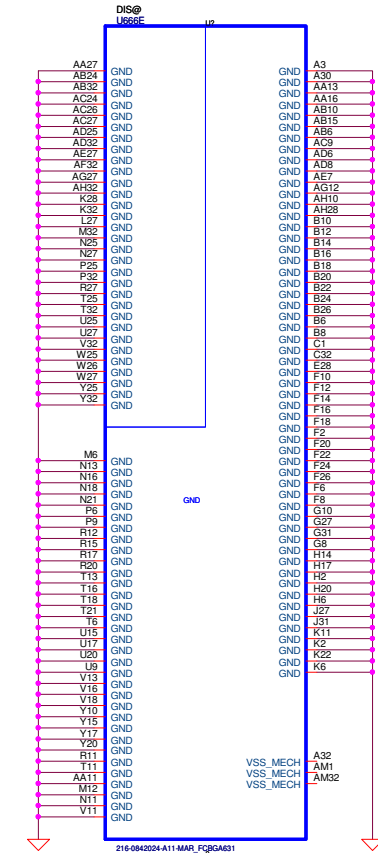
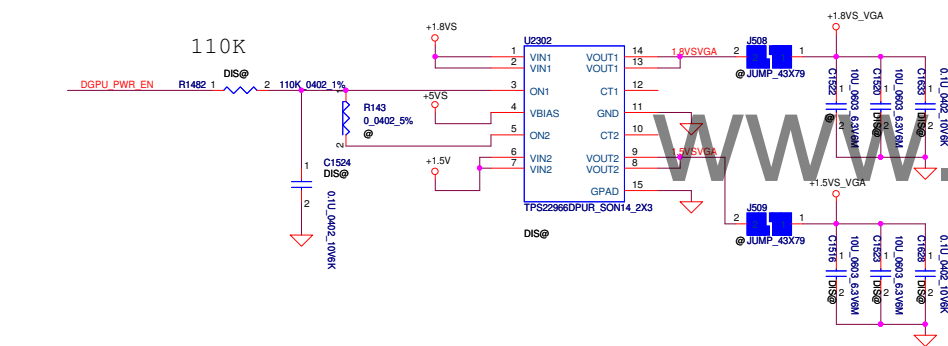


Memory ID	Memory Type	Configuration	Size
1	gDDR3-2133	Samsung K4W2G1646E-BC1A	2Gb X4 (256GBX4)
		SA000068U00 - S IC D3 128MX16 K4W2G1646E-BC1A FBGA 96P	
2	gDDR3-2000	Micro MT41J128M16JT-093G	2Gb X4 (256GBX4)
		SA000067500 - S IC D3 128M16 MT41J128M16JT-093G:K FBGA	

EX:
PS_3=11001 (PU=NC, PD=4.75K, C=NC) for Samsung 1GB
PS_3=11010 (PU=8.45K , PD=2K, C=NC) for Micro 1GB



+1.8VS TO +1.8VS_VGA
+1.5V TO +1.5VS_VGA

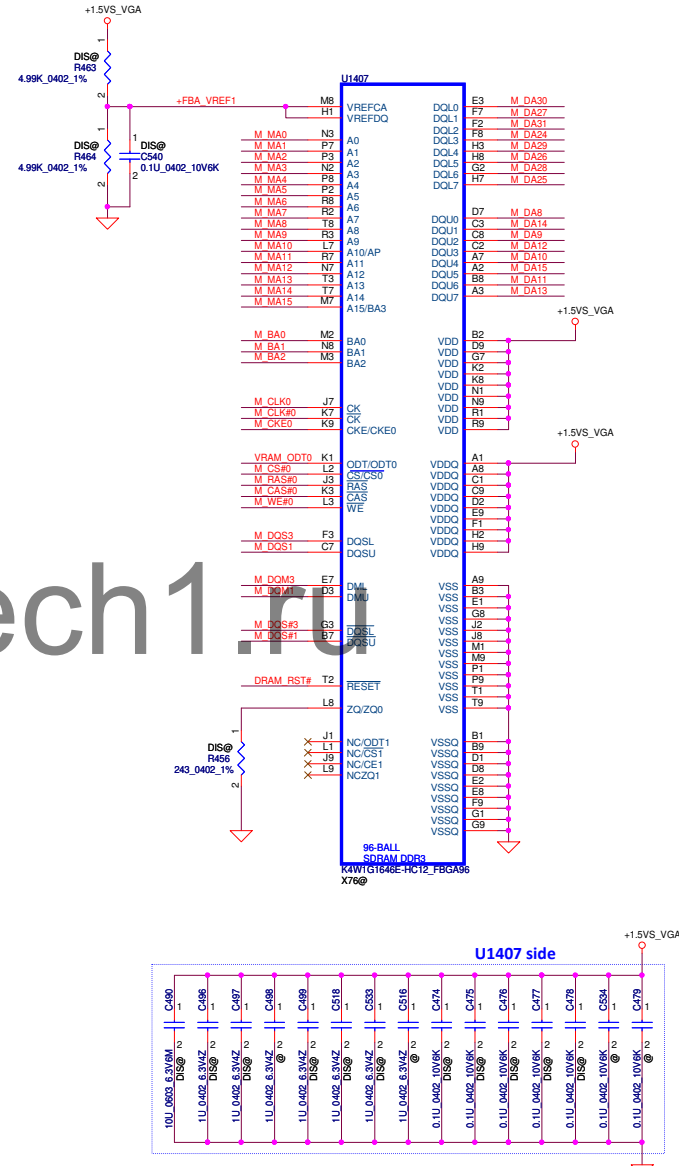
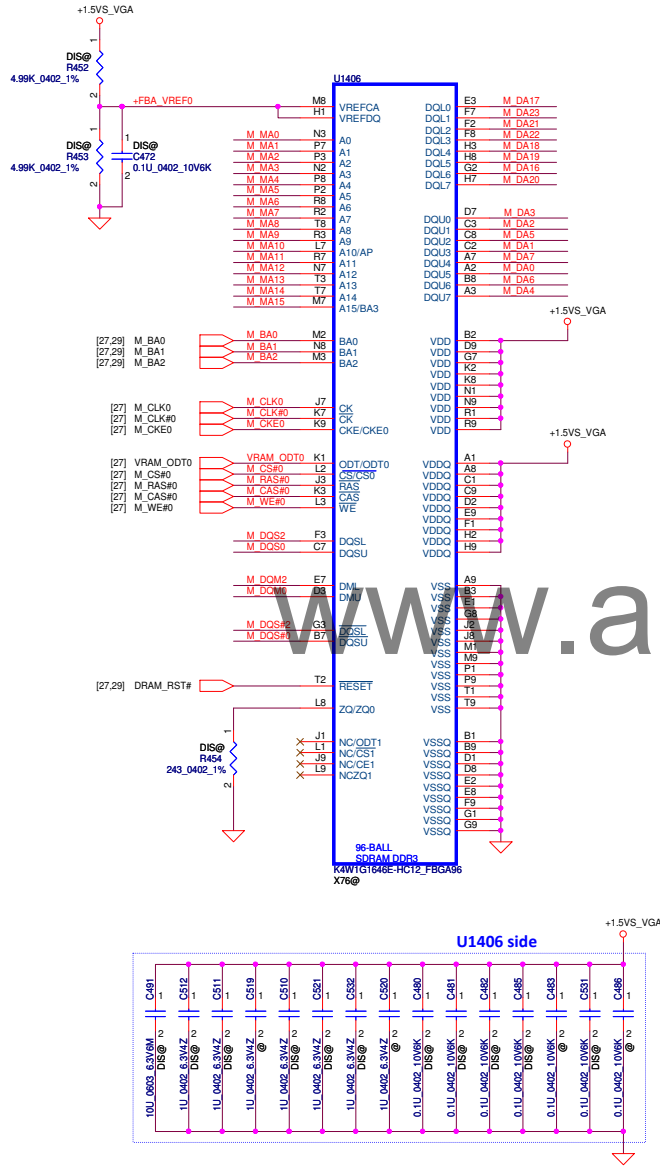


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				Custom	LA-9611P	0.4
				Date: Tuesday, February 26, 2013		Sheet 25 of 53

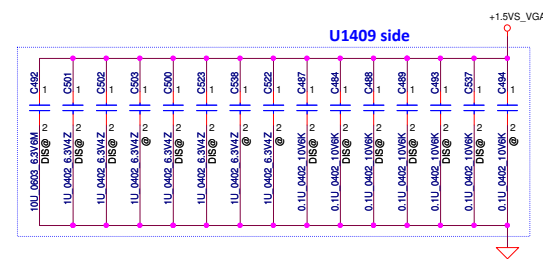
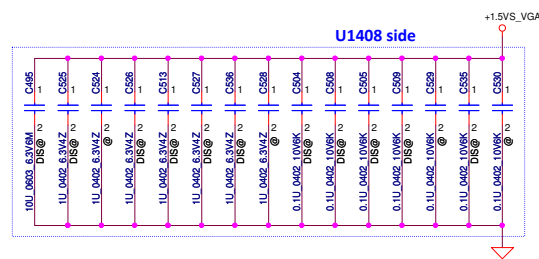
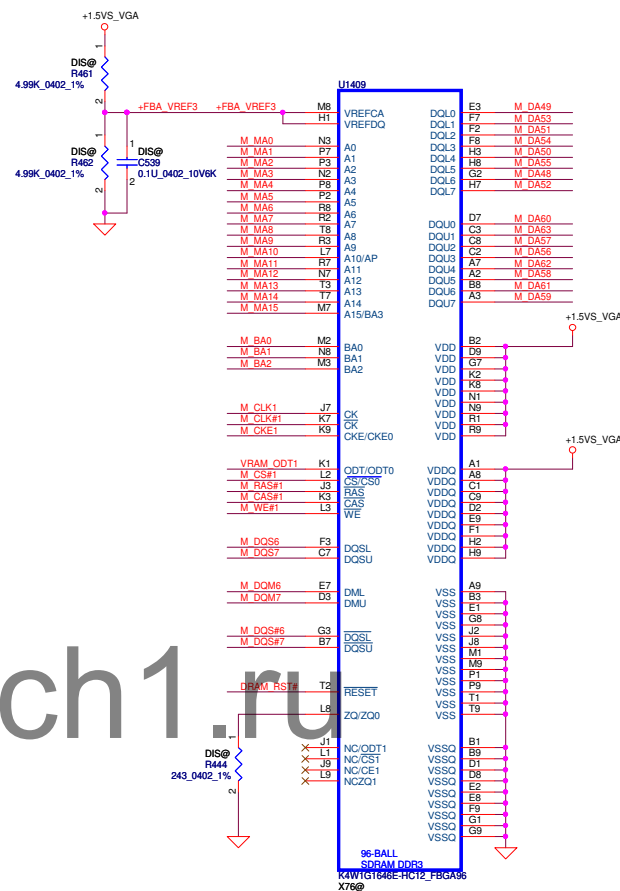
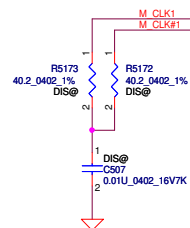
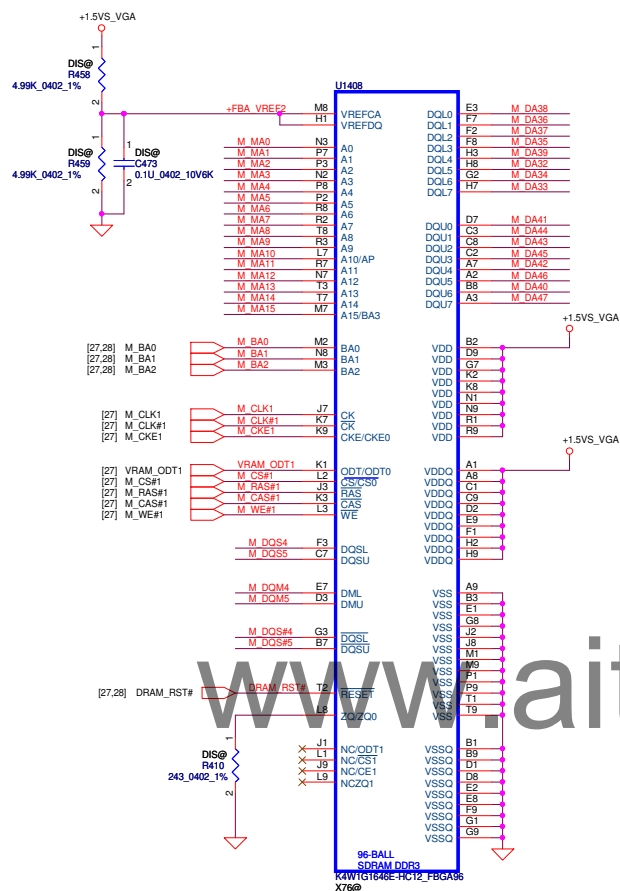
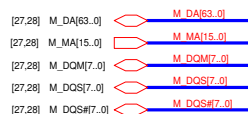
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Size	<div>Document Number</div> <div>LA-9611P</div> <div>Rev 0.4</div>
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Memory Partition A - Lower 32 bits

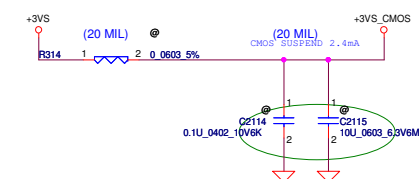
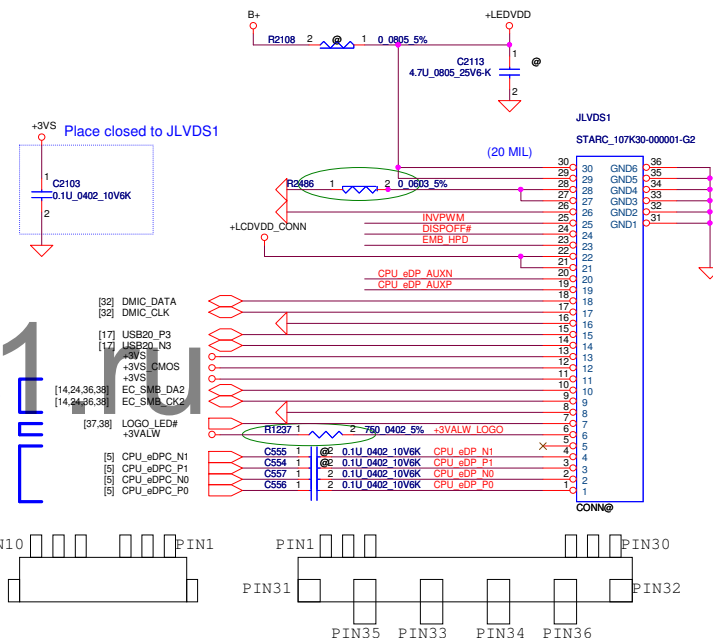
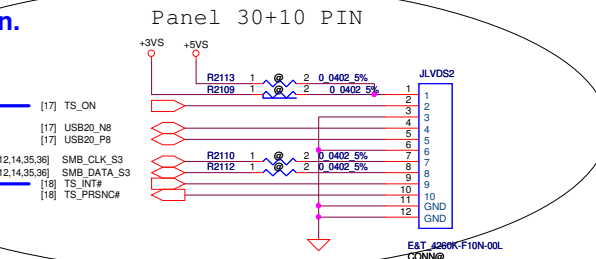
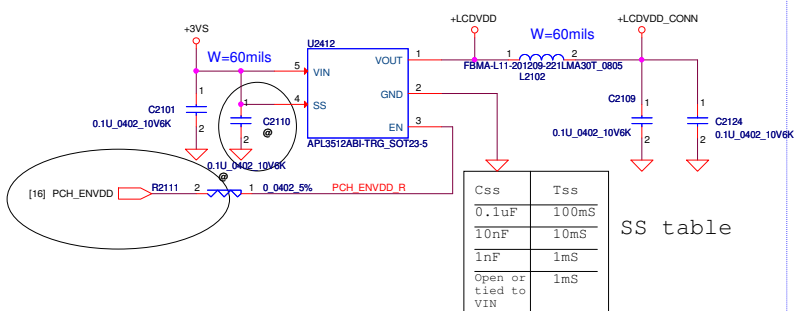
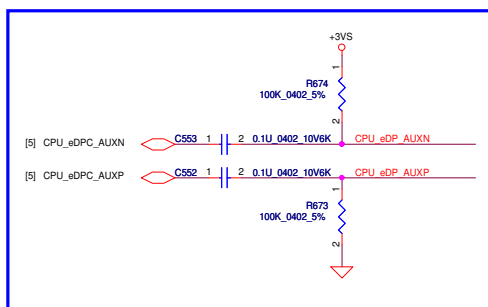
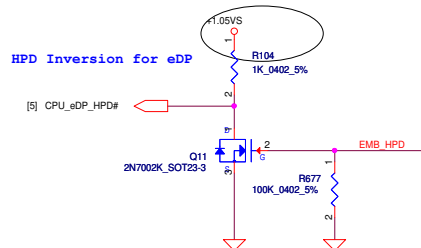
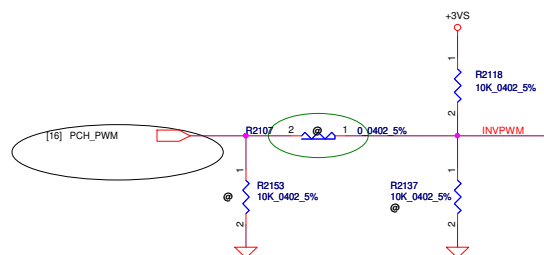
- [27:29] M_DA[63:0] M_DA[63:0]
- [27:29] M_MA[15:0] M_MA[15:0]
- [27:29] M_DQM[7:0] M_DQM[7:0]
- [27:29] M_DQS[7:0] M_DQS[7:0]
- [27:29] M_DQS# [7:0] M_DQS# [7:0]



1	2
Memory Partition A - Upper 32 bits	



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				Custom	LA-9611P	
				Date:	Tuesday, February 26, 2013	Rev 04
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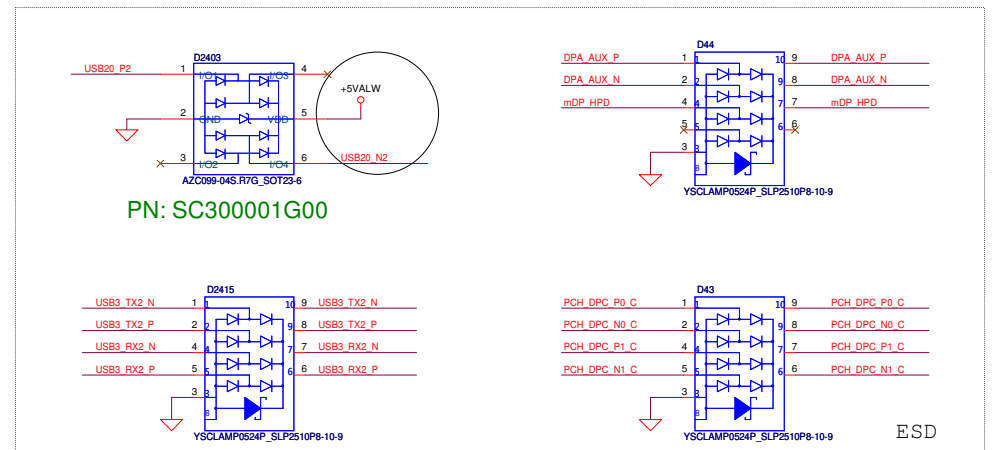


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

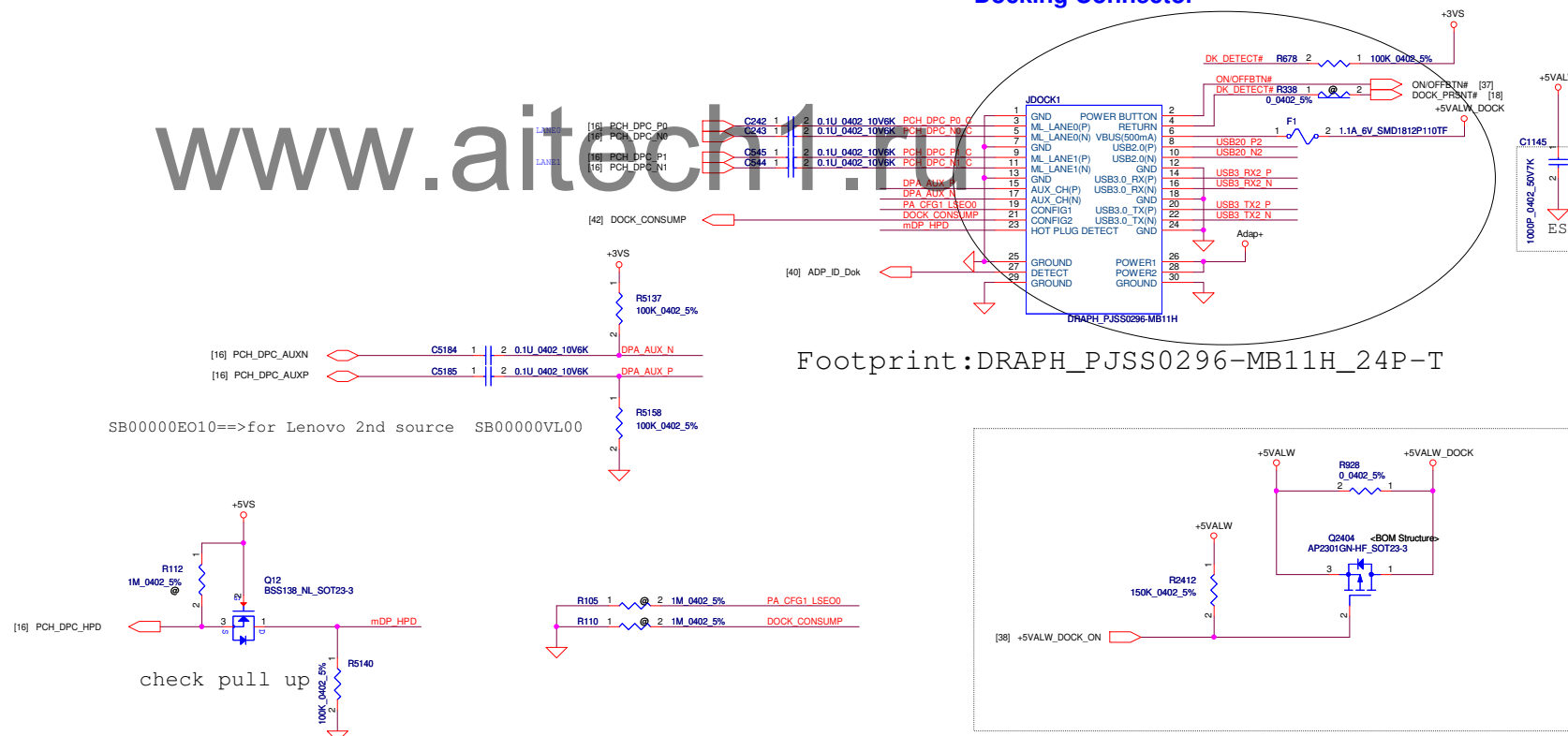
Security Classification		Compal Secret Data		<div>Compal Electronics, Inc.</div> <div>Title</div> <div>LVDS Connector</div>	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Size Custom	<div>Document Number</div> <div>LA-9611P</div> <div>Rev 0.4</div>
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Docking (USB3.0)

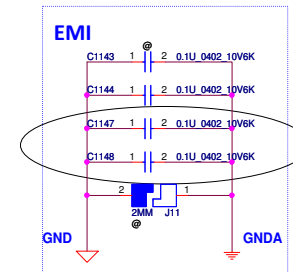


Docking (Display Port)

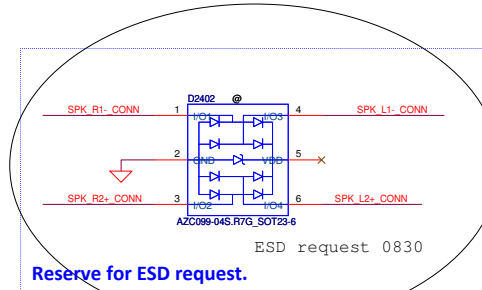
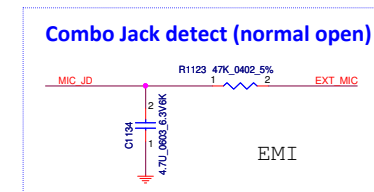
Docking Connector



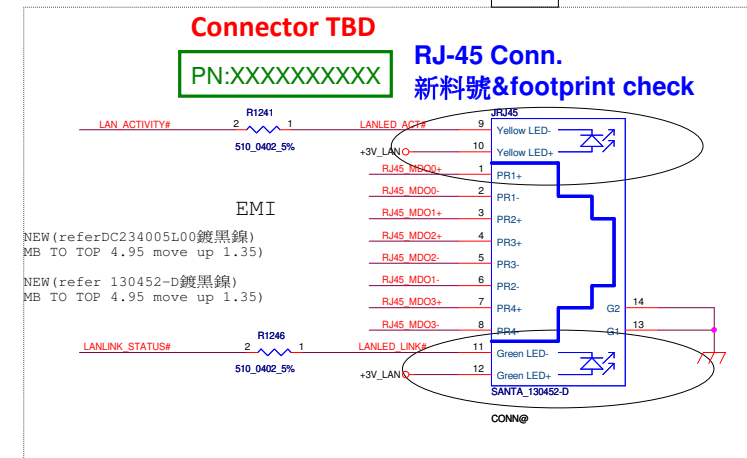
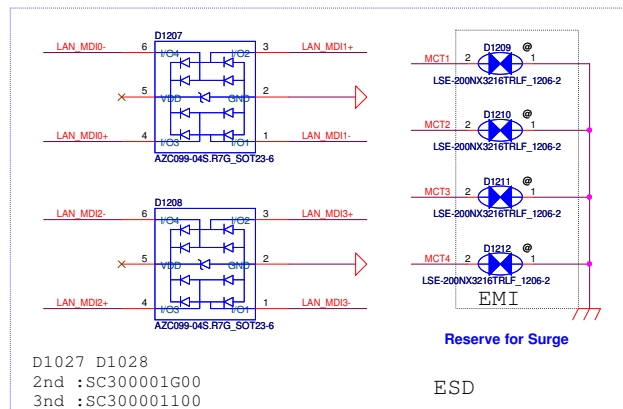
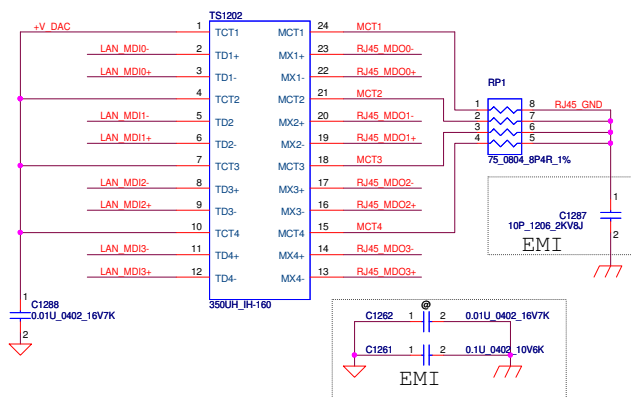
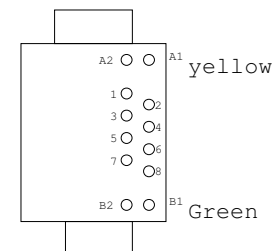
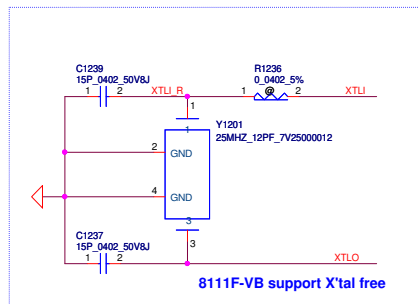
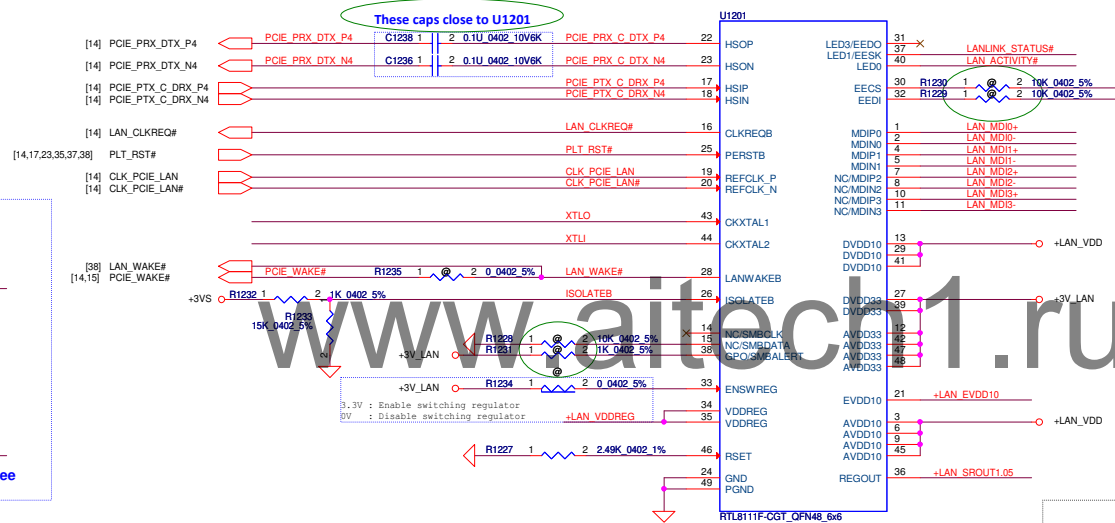
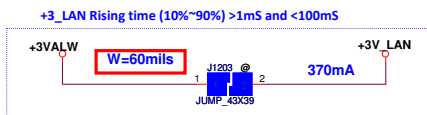
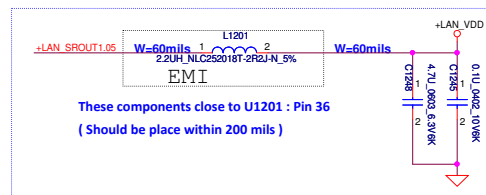
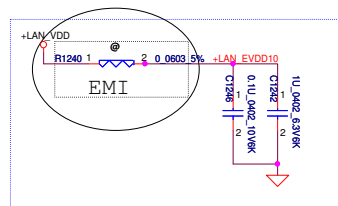
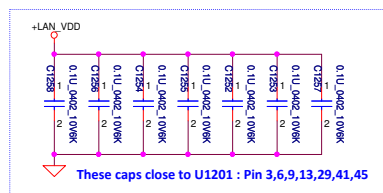
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	Docking
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Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in

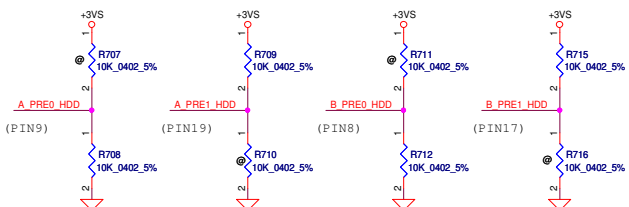
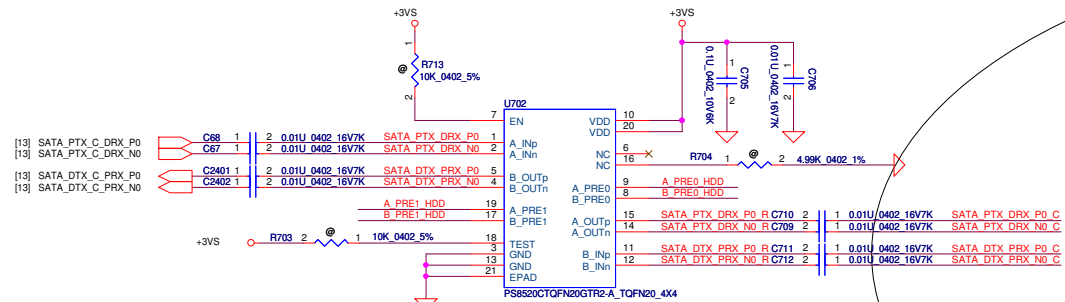


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				Audio Codec ALC3202	
				Size	Document Number
				LA-9611P	Flow 0.
Date		Tuesday, February 26, 2013		Sheet	32 of 53



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				Custom	LA-9611P	0.4
				Date:	Wednesday, February 27, 2013	Sheet 33 of 53

SATA HDD BTB CONN.



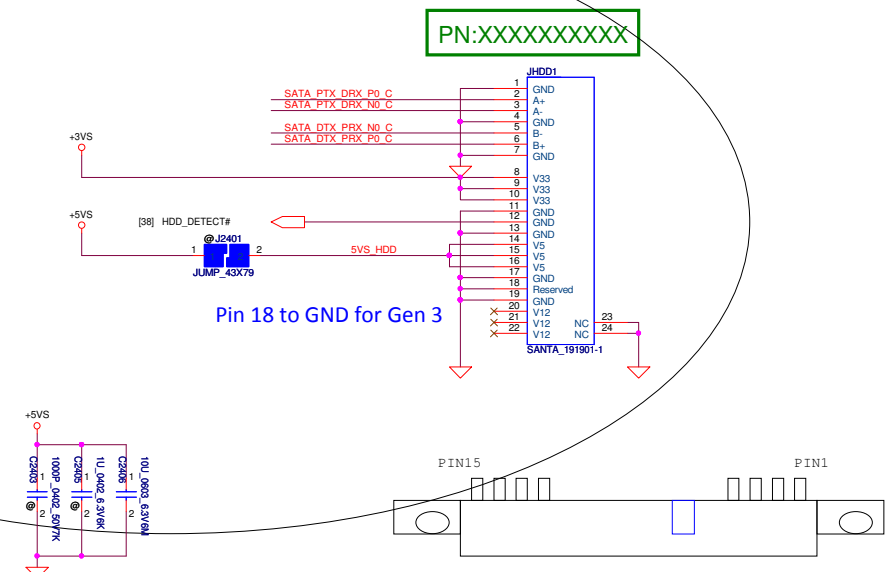
	TEST (Internal pull Low)
Normal operation (default)	Low
Compliance testing mode enable	High

	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High

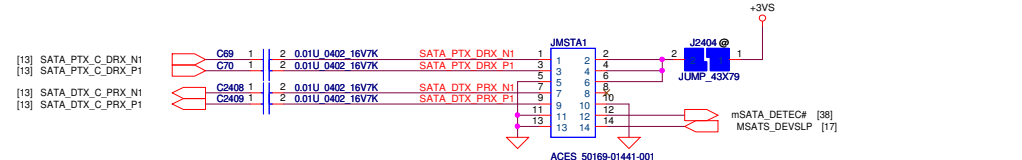
D	C	E	D
0	6	0	0
1	3	7	4

EN	Device Function-> StandBy Mode
0	D
1	C

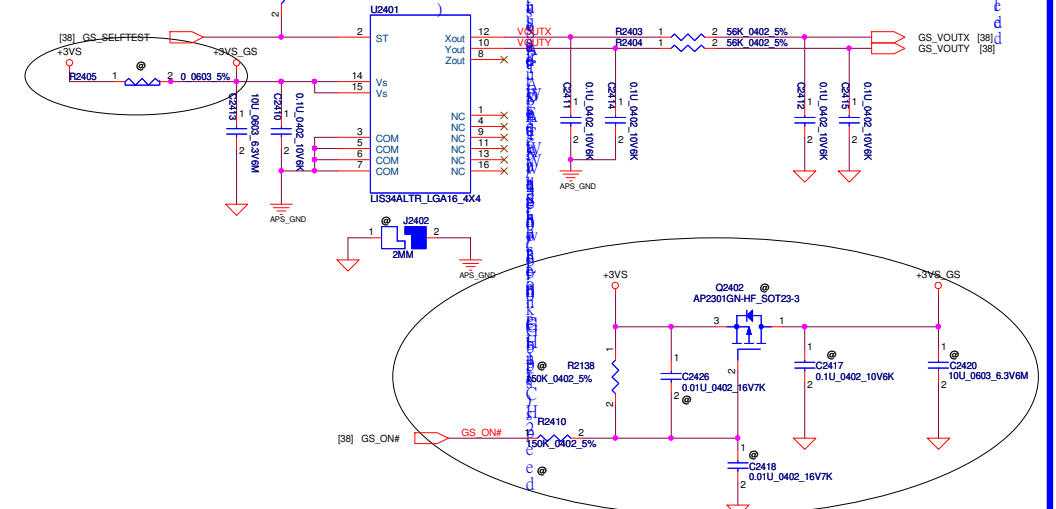
SATA HDD CONN.



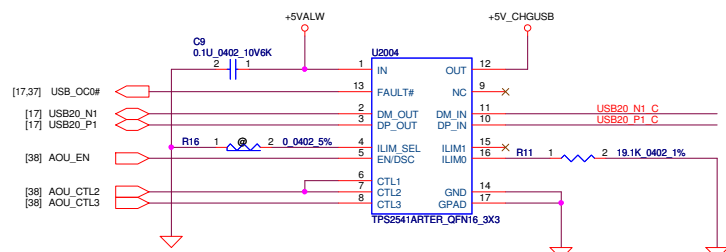
mSATA CONN.



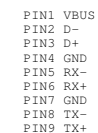
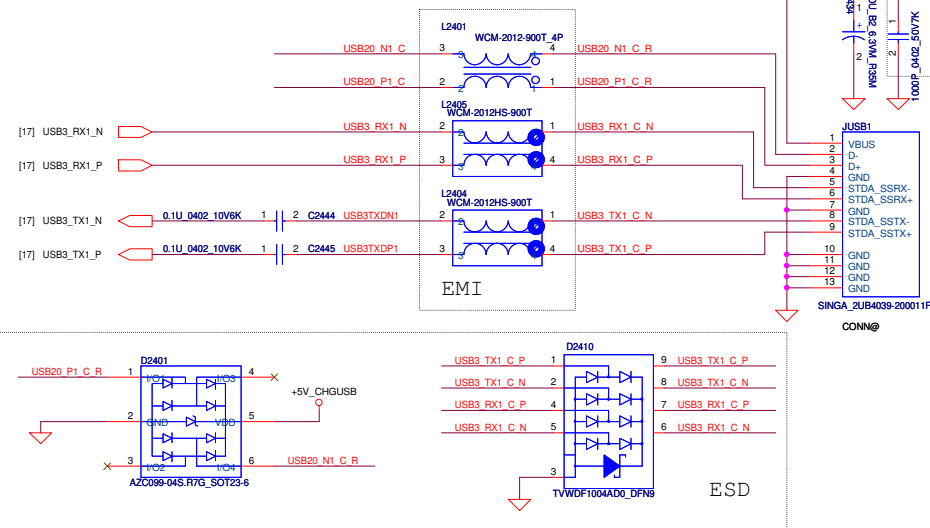
APS G-Sensor



USB 3.0 Charger & Conn.

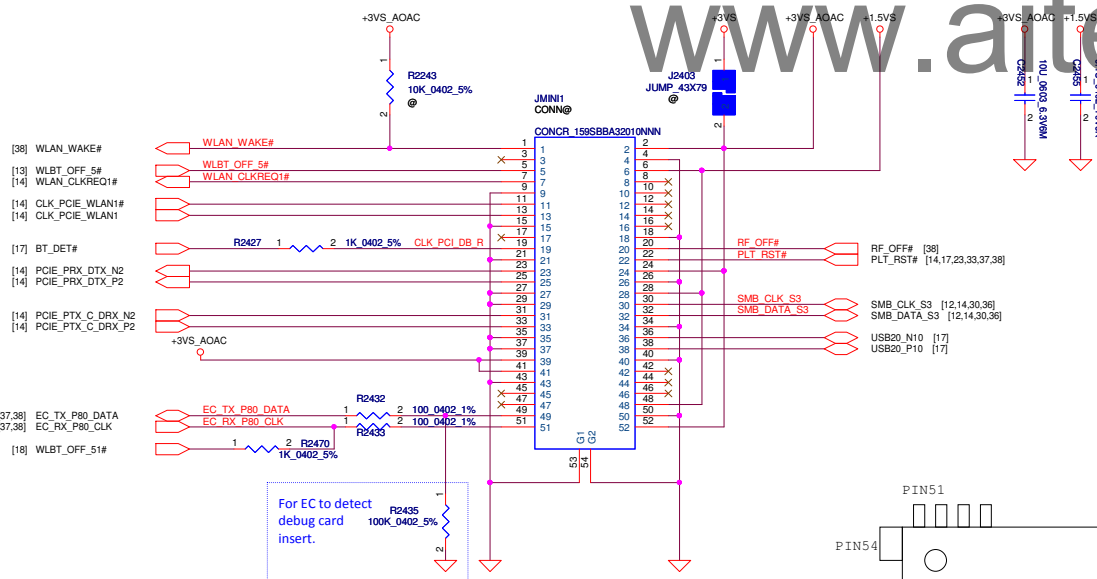


Superworld's common mode choke(SM070001V00) has quality issue for USB 3.0



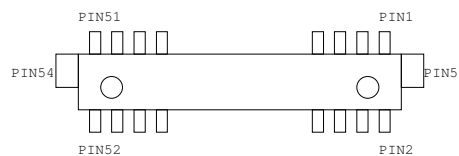
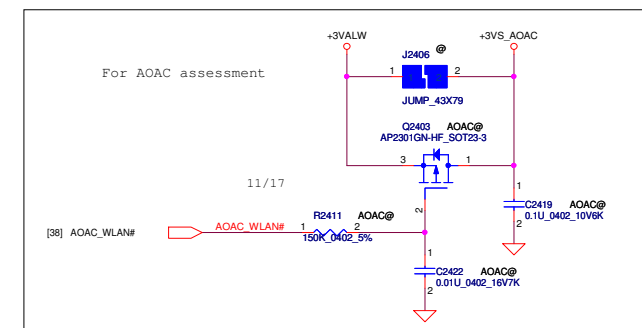
Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



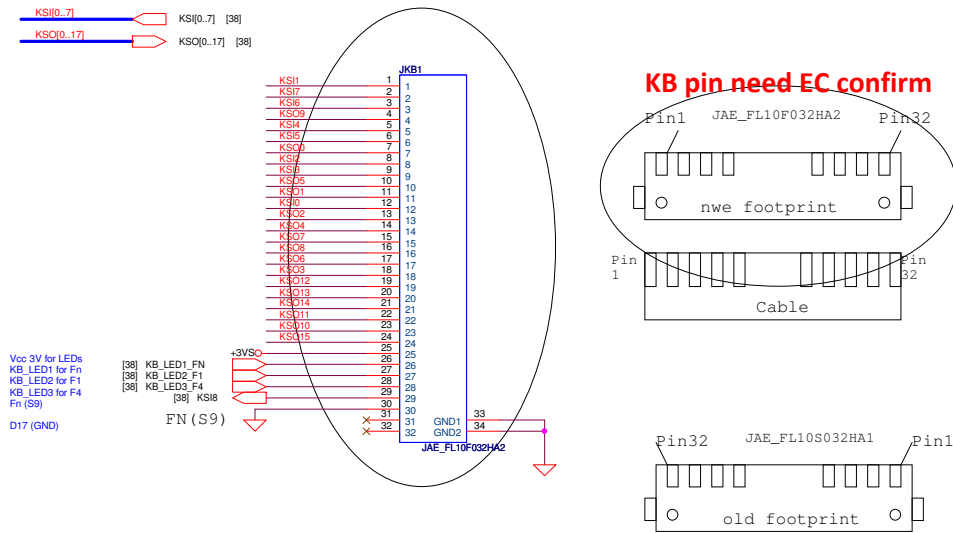
NEW(apply compal PN)
159SBBA32010NNN

Need check WLAN/BT module OFF pin

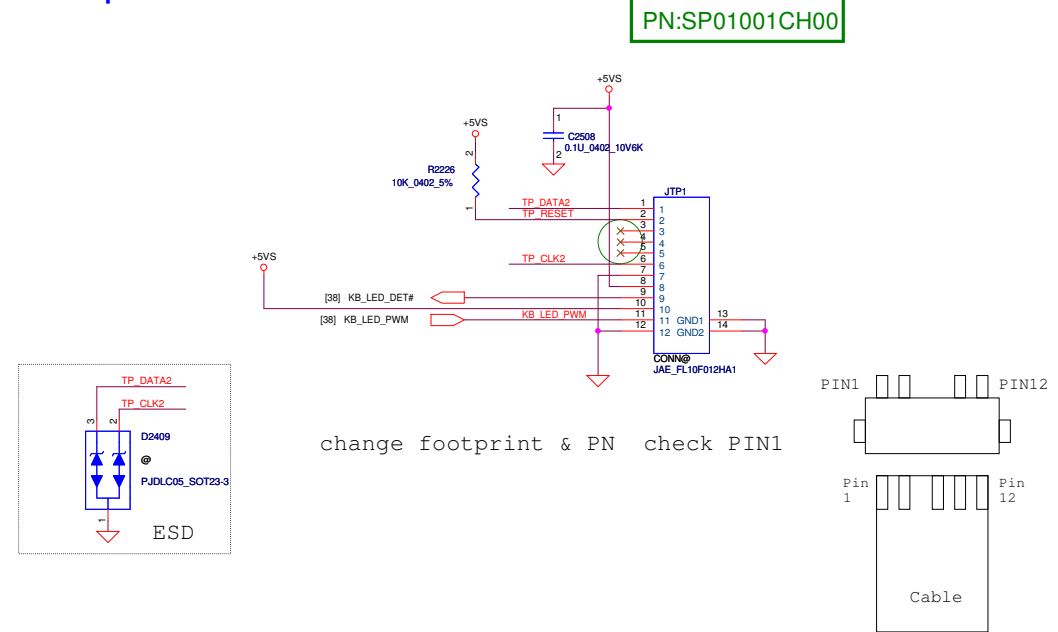


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					LA-9611P	0.
				Date:	Tuesday, February 26, 2013	Sheet 35 of 53

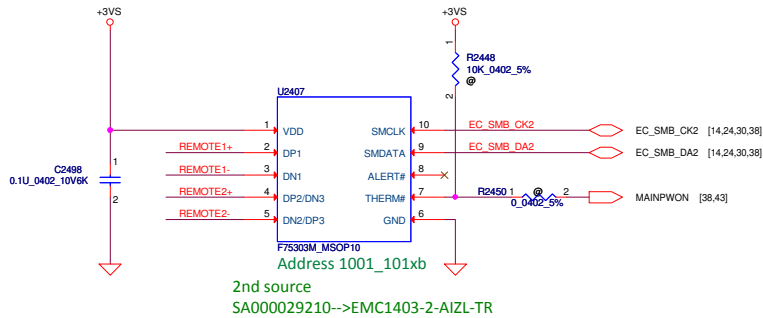
INT_KBD Conn.



Track point

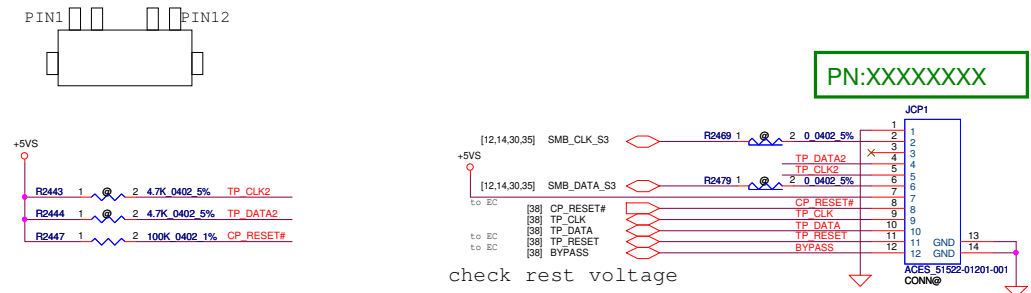


Fintek thermal sensor placed near CPU Core

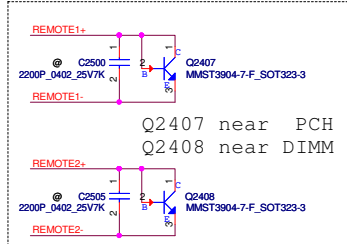
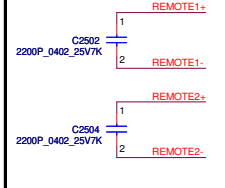


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Click pad



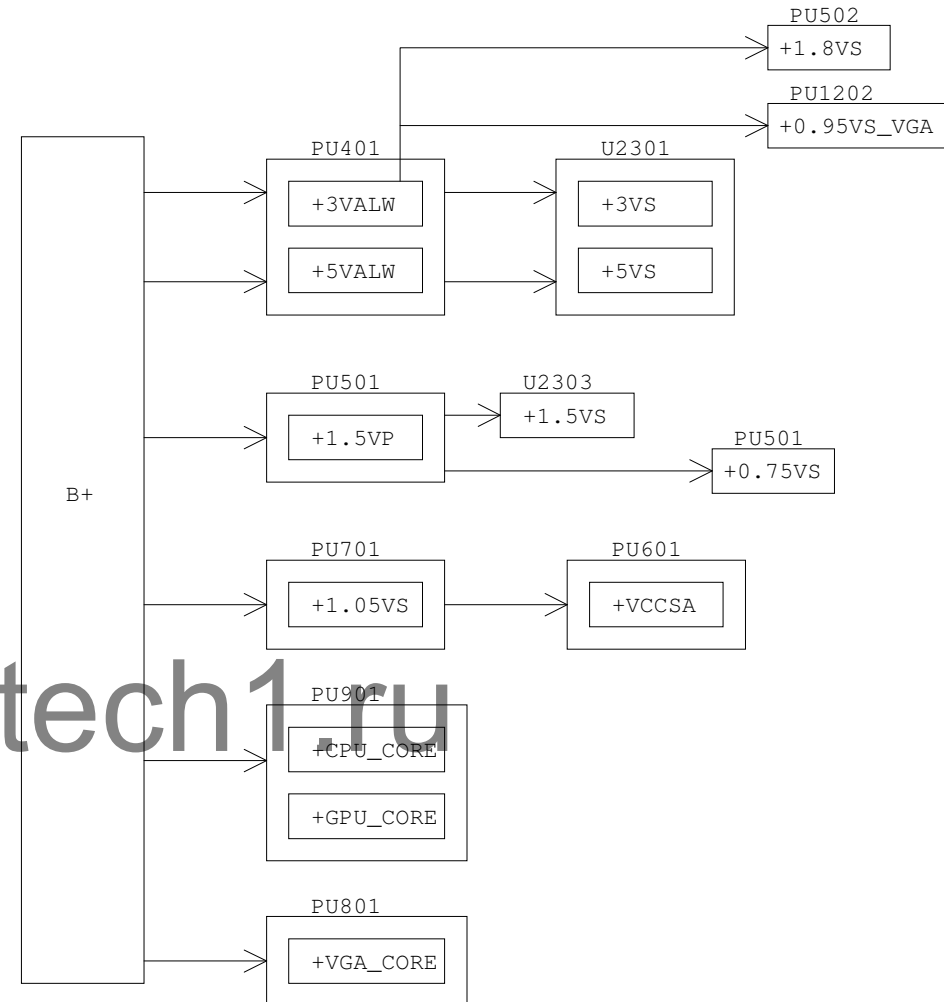
Close U2407



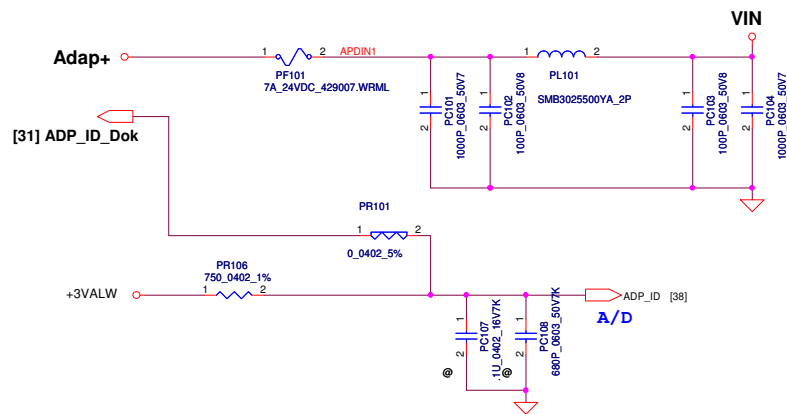
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	KB/CP/TP/FP/Thermal Sensor	Rev 04
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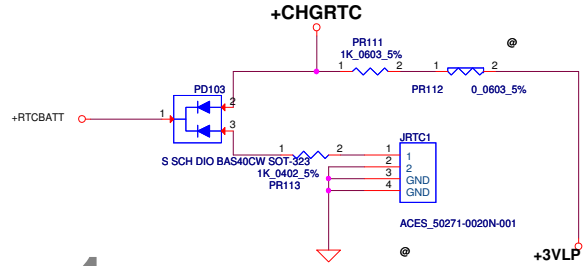
[illegible][illegible]

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				Custom	0.4
				Date: Tuesday, February 26, 2013 Sheet 39 of 53	

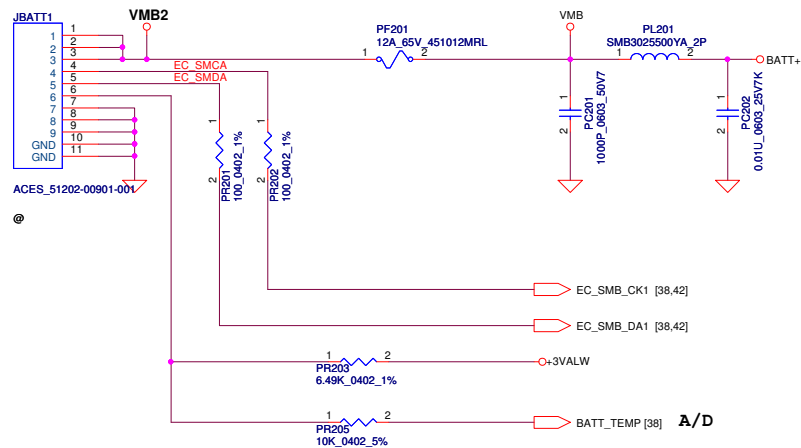


ADP_ID

AC Adapter	45W	65W	90W	135W
R(ohm)	118	287	549	1000
ADP_ID(V)	0.449	0.913	1.395	1.886
Detection	<=0.663, <=1.134, <=1.618, <=2.109,			
-Voltage(V)	>0.234 >0.693 >1.172 >1.663			



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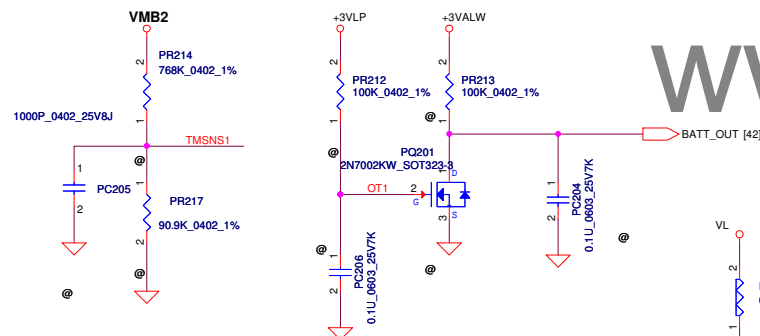
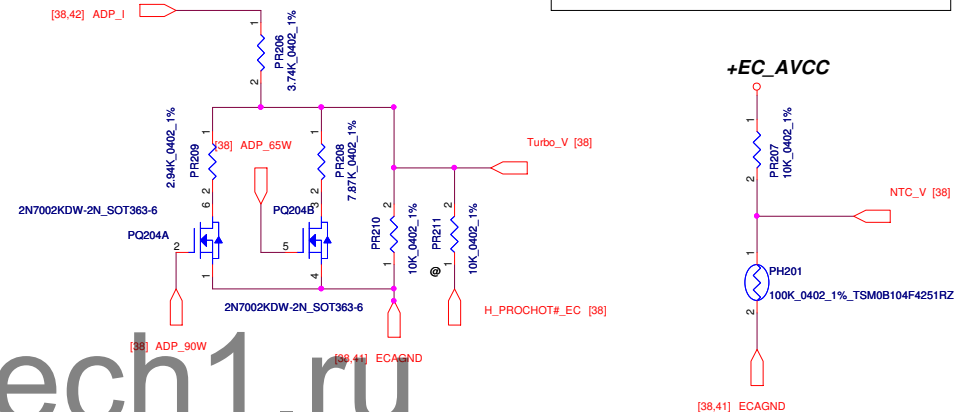
Resistance between Turbo_V and ECAGND:

45 W: 10K (Default)
 65 W: 4.4K (ADP_65W to High, ADP_90W to Low)
 90 W: 2.27K (ADP_90W to High, ADP_65W to Low)

Trigger Power:

45 W → 55 W → ADP_I:1.65
 65 W → 74 W → ADP_I:2.22
 90 W → 106 W → ADP_I:3.18

PH201 under CPU bottom side :
 CPU thermal protection at 100 degree C

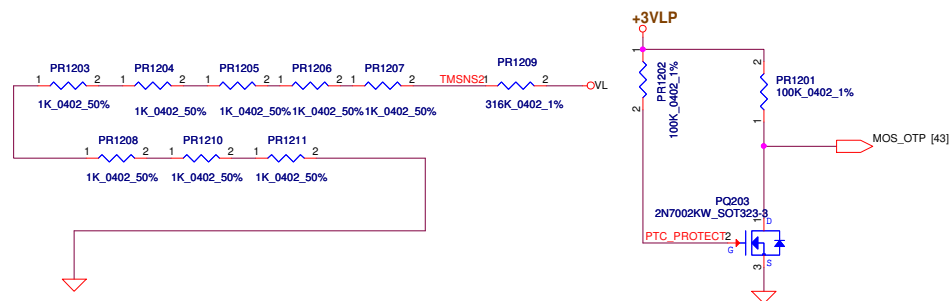


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PH201:

Temp.	Rman.	Rnor.	Rmin. (Kohm)
93	7.3419	7.0792	6.8253

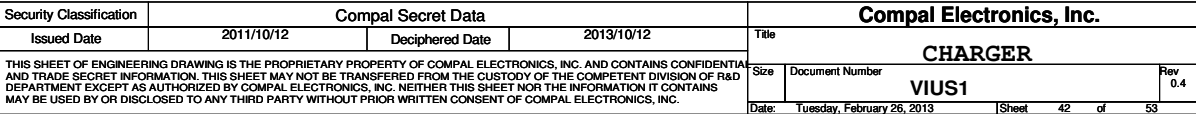
Posestor

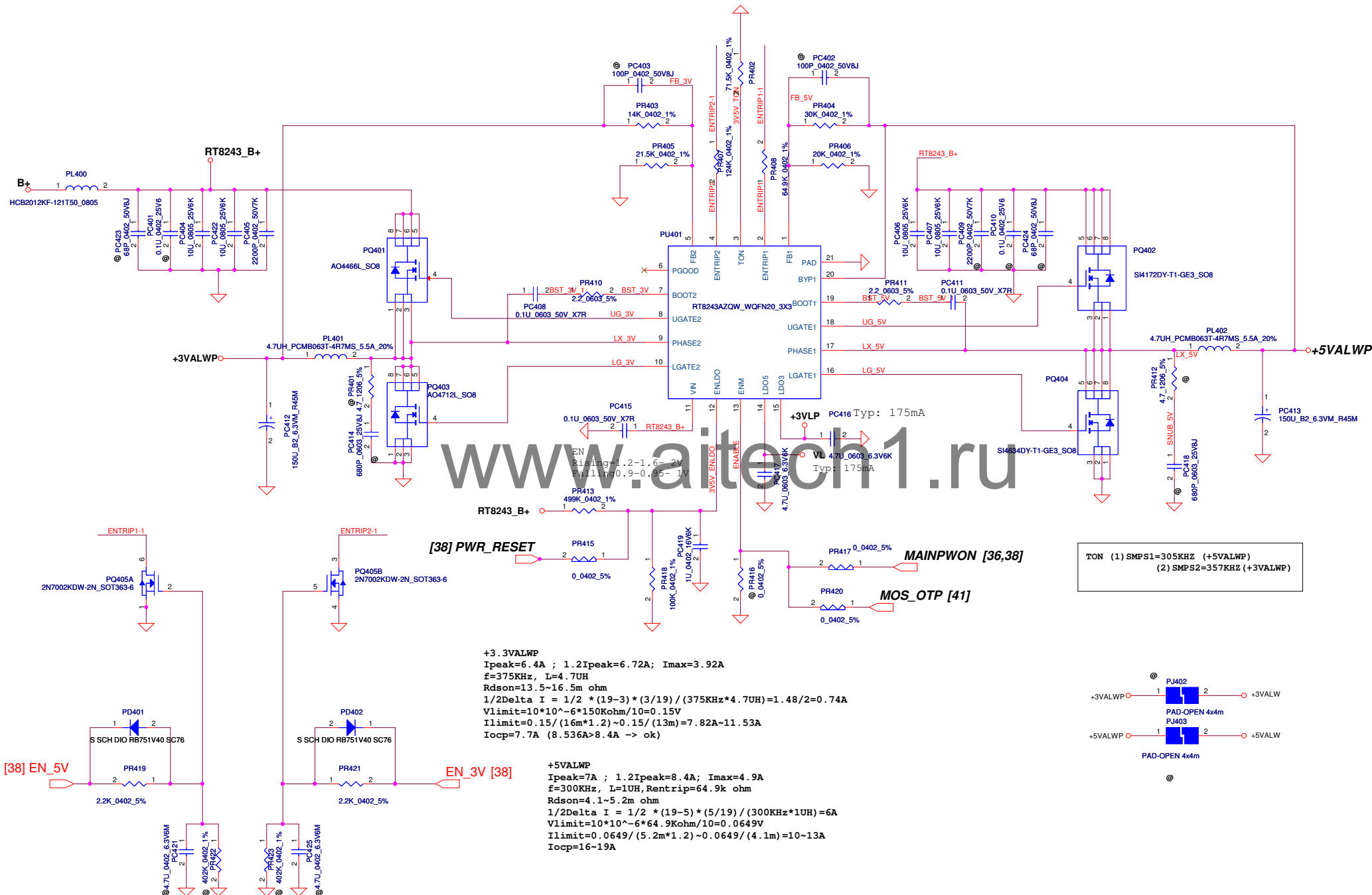


MOS_OTP:
 Default:High
 Active :Low

PTC_PROTECT:
 Default:Low
 Active :High

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/01/25				Title			
				Deciphered Date				PWR-BATTERY CONN/OTP			
				2010/12/31				VIUS1			
								Rev 0.4			
								Date: Tuesday, February 26, 2013			
								Sheet 41 of 53			

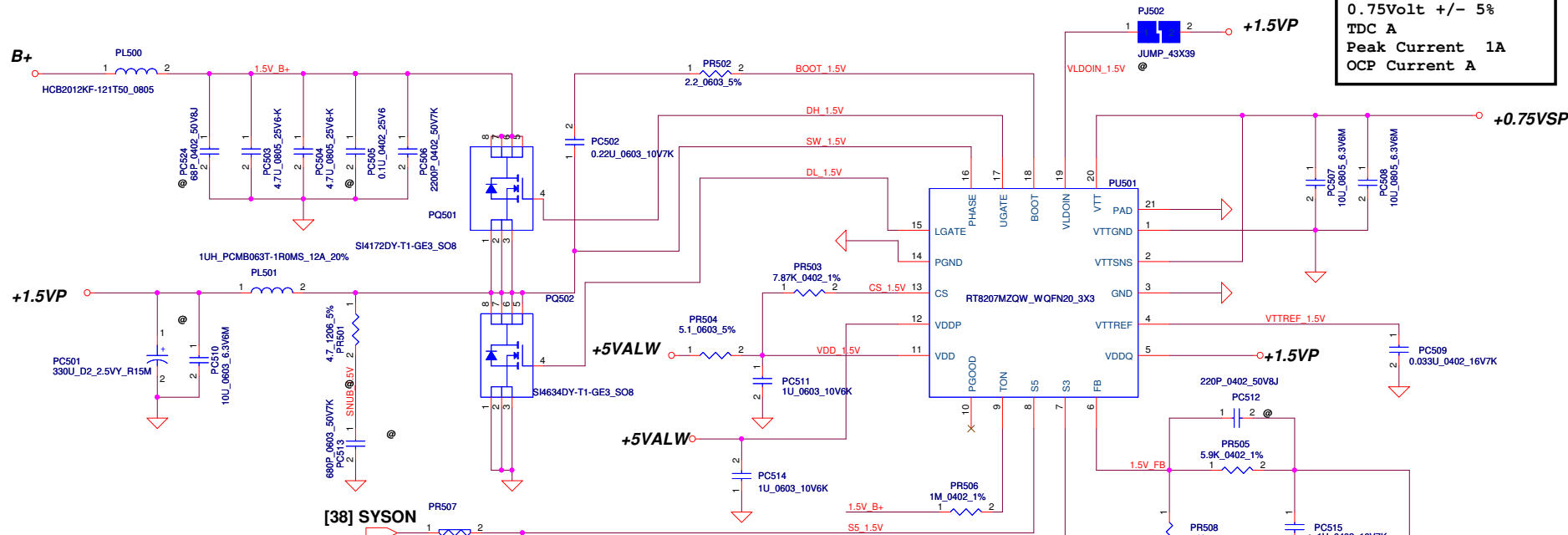




2012/10/19
check the EN circuit

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				VIUS1	0.4
Date: Tuesday, February 26, 2013				Sheet	43 of 53

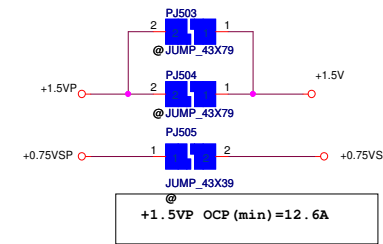
0.75Volt +/- 5%
TDC A
Peak Current 1A
OCP Current A



1.5VP
TDC A
Peak Current 11.027 A
OCP current 13.36~18.27 A
TYP MAX
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :2.6mohm , 3.2mohm

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

(Discharge) (Discharge) (Discharge)

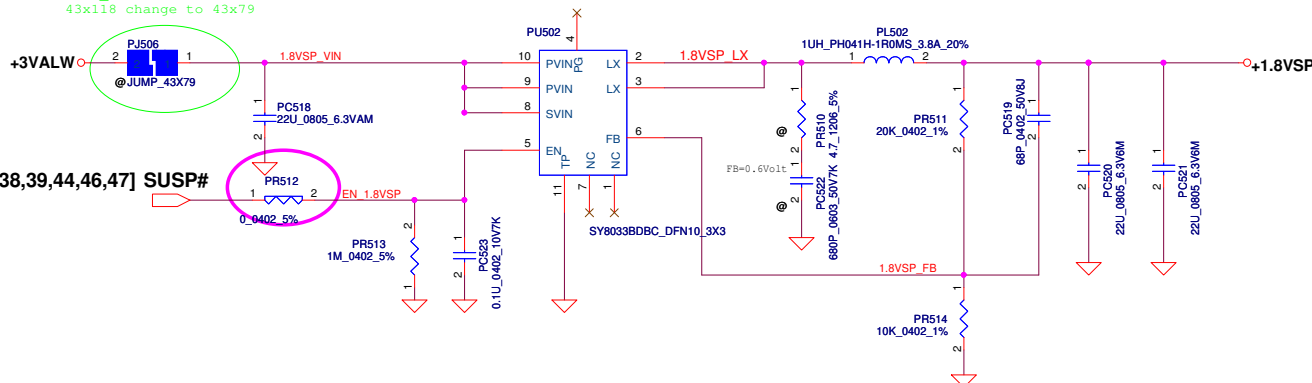


+1.5VP OCP (min)=12.6A

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PR509 change for BW power sequence 10/17/2012

2011_0801 JP504 form
43x118 change to 43x79



2011_0801 JP505 form
43x118 change to 43x79



1.8VSP max current=4A

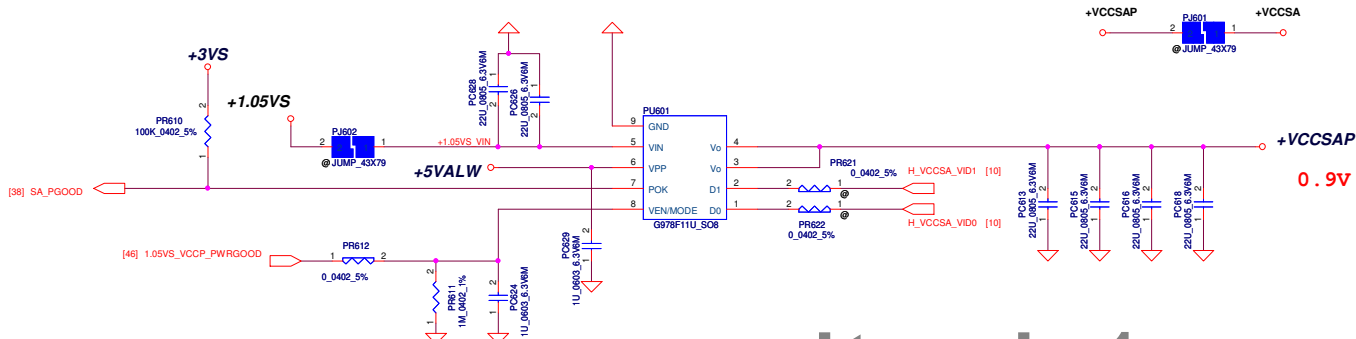
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+1.8VSP
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VID [0]	VID [1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

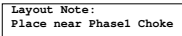
+VCC_SAP
TDC 2.9A
Peak Current 4A
OCP current 5.4A

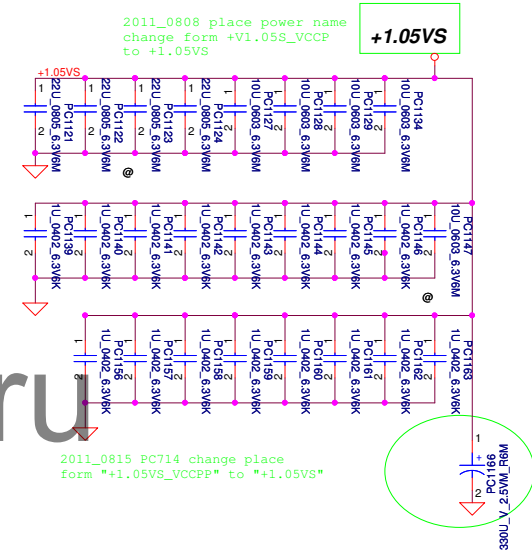
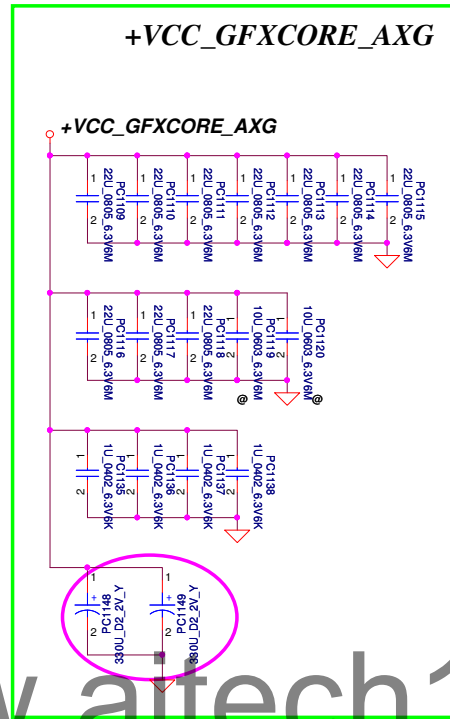
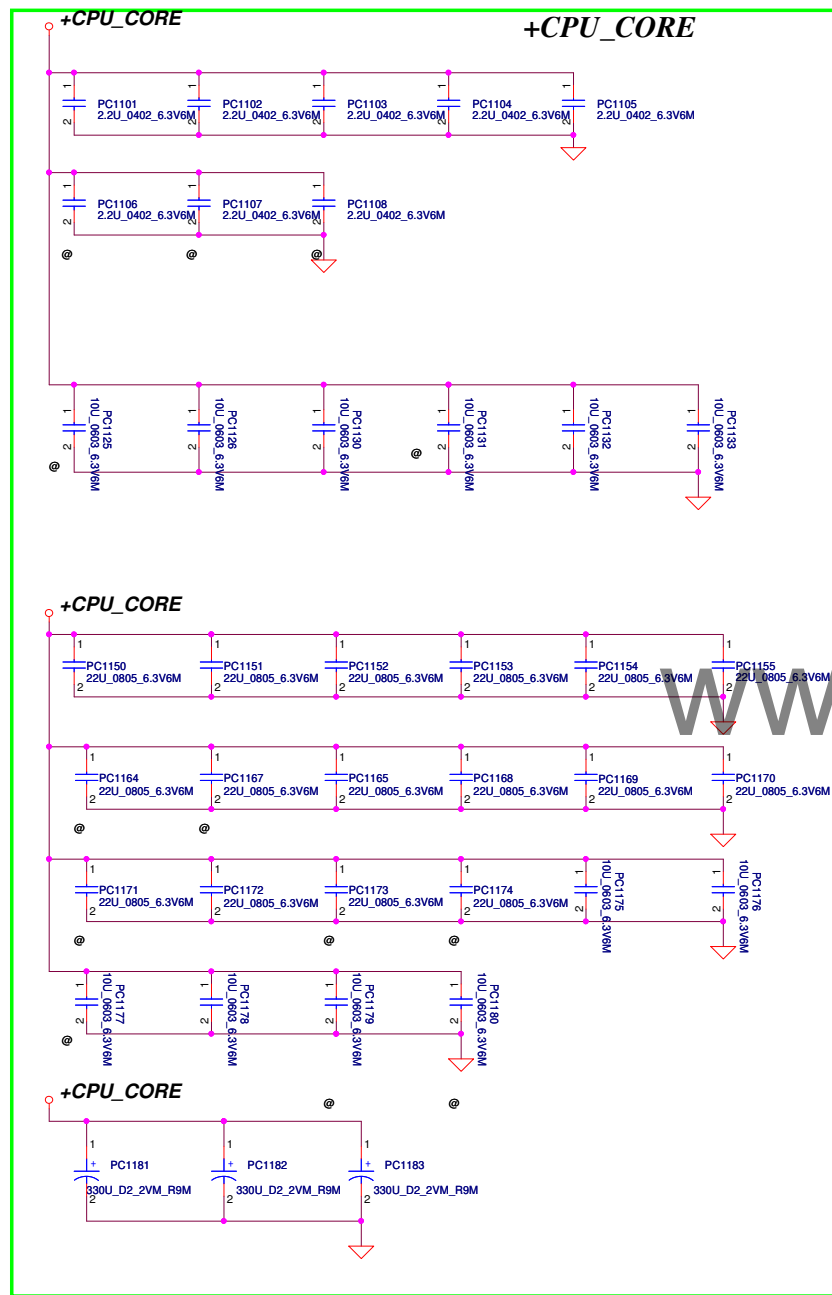
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



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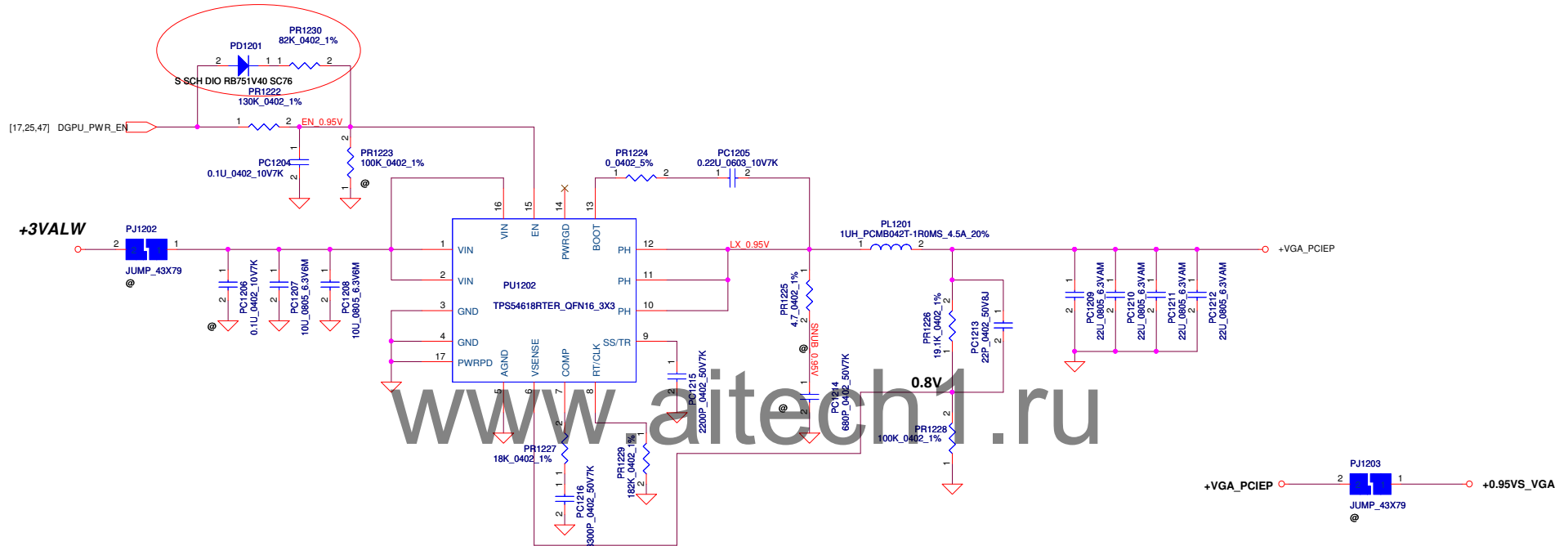
Default





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PR1230,PD1201 add for HW power sequence required 10/31/2012



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				Sheet	51 of 53
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Item	Reason for change	PG#	Modify List	Date	Phase
1				2012/06/05	
2				2012/06/08	
3				2012/06/08	
4				2012/06/08	
5					
6					
7					
8					
9					
10					
11					
12					
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14					
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				Size	Document Number
				Custom	VIUS1
Date: Tuesday, February 26, 2013				Rev	0.4
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power

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		2012/07/01		Title	
				PIR (EE)	
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		Date		Tuesday, February 28, 2012	
		Sheet		53 of 53	